KT0937-D8 Programming Guide

Common Settings

1 Power up procedure of KT0937-D8

1) Reading register 0x02 to judge whether KT0937-D8 have been power-on.
2) Entry standby mode if KT0937-D8 has been power-on.
3) Waking up, when it need.
4) Initialization KT0937-D8.
5) Setting band.
6) Setting volume.
7) Power-on finish.

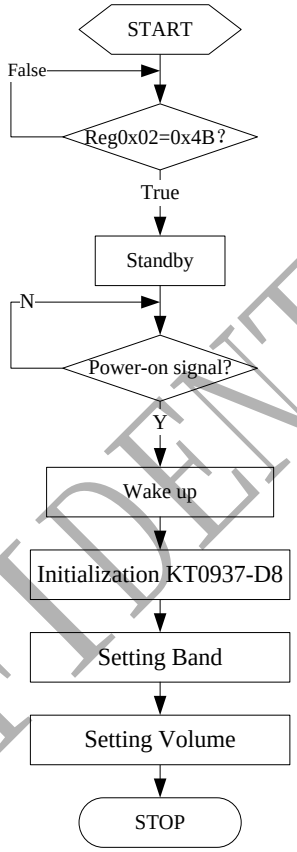


Figure 1: Flow chart of power-up

2 How to initialize KT0937-D8

It must follow the procedure to initialize KT0937-D8:

1) Setting DEPOP_TC<2:0> register.
2) Setting AUDV_DCLVL<2:0> register.
3) Initializing the system clock.
4) When the POWERON_FINISH flag was 1, the register is to be written in the following order:
5) Initializing audio registers.
6) Setting FLT_SEL<2:0> register.
7) Initializing FM AFC registers.
8) Initializing AM AFC registers.
9) Initializing AM_BBAGC registers.
10) Initializing FM valid station registers.
11) Initializing AM valid station registers.
12) Initializing Blend and mono registers.

13) Setting De-emphasis time constant.
14) Initializing FM softmute registers.
15) Initializing AM softmute registers.
16) Setting FM_RFGAIN_LIMIT_EN to 1.
17) Setting ANT_CALI_SWITCH_BAND to 1.
18) Setting AM_SUP_ENHANCE to 1.
19) Setting AM_SEL_ENHANCE to 1.
20) Configuration of initializing interrupt output pin

Registers	Address	Default Value	Access	Recommended Value
DEPOP_TC<2:0>	0x4E<5:4>	3	Read/Write	3
AUDV_DCLVL<2:0>	0x4E<2:0>	2	Read/Write	2
POWERON_FINISH	0x1B<2>	0	Read Only	-
FLT_SEL<2:0>	0x62<2:0>	1	Read/Write	1
FM_RFGAIN_LIMIT_EN	0x24<7>	1	Read/Write	1
ANT_CALI_SWITCH_BAND	0x2F<5>	0	Read/Write	1
AM_SUP_ENHANCE	0x2F<2>	0	Read/Write	1
AM_SEL_ENHANCE	0x2F<0>	0	Read/Write	1

3 How to set the system clock of KT0937-D8

The system clock initialization step is as the following:

1) Setting DIVIDERP<10:0>.
2) Setting DIVIDERN<10:0>.
3) Setting FPFD<19:0>.
4) Setting RCLK_EN.
5) Setting SYSCLK_CFGOK to 1.

Registers	Address	Default Value	Access	Recommended Value[1]
DIVIDERP<10:8>	0x04<2:0>	0	Read/Write	0
DIVIDERP<7:0>	0x05<7:0>	1	Read/Write	1
DIVIDERN<10:8>	0x06<2:0>	2	Read/Write	2
DIVIDERP<7:0>	0x07<7:0>	0x9C	Read/Write	0x9C
FPFD<19:16>	0x08<3:0>	8	Read/Write	8
FPFD<15:8>	0x09<7:0>	0	Read/Write	0
FPFD<7:0>	0x0A<7:0>	0	Read/Write	0
RCLK_EN	0x0D<4>	0	Read/Write	0
SYSCLK_CFGOK	0x04<7>	0	Read/Write	1
NOTE：Use 32.768KHz Crystal				

4 How to use I2C interface

1) MCU is a master device. KT0937-D8 is a slave device.
   - ✧ CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (Figure 2). Data changes during SCL high periods will indicate a start or stop condition as defined below.
   - ✧ START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command. (Figure 3).
   - ✧ STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode. (Figure 3Figure 3: Clock and Data Transitions).

ACKNOWLEDGE: Data transfer with acknowledge is obligatory. The acknowledge-related clock pulse is clock pulse is generated by the master (MCU).MCU releases the SDA line (HIGH) during the

acknowledge clock pulse. KT0937-D8 must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW. (Figure 4Figure 4: Acknowledge

✧).

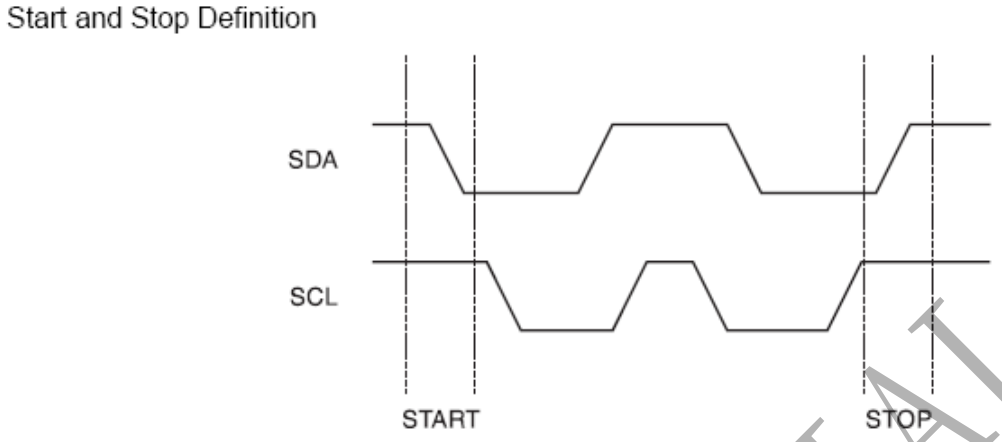


Figure 2: Start and Stop Definition

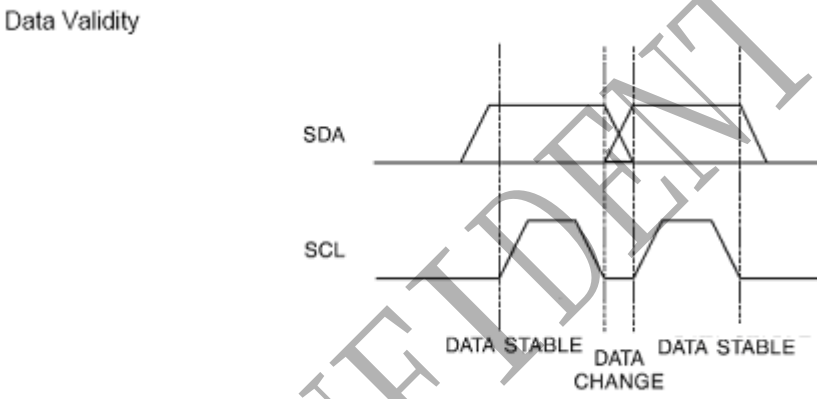


Figure 3: Clock and Data Transitions

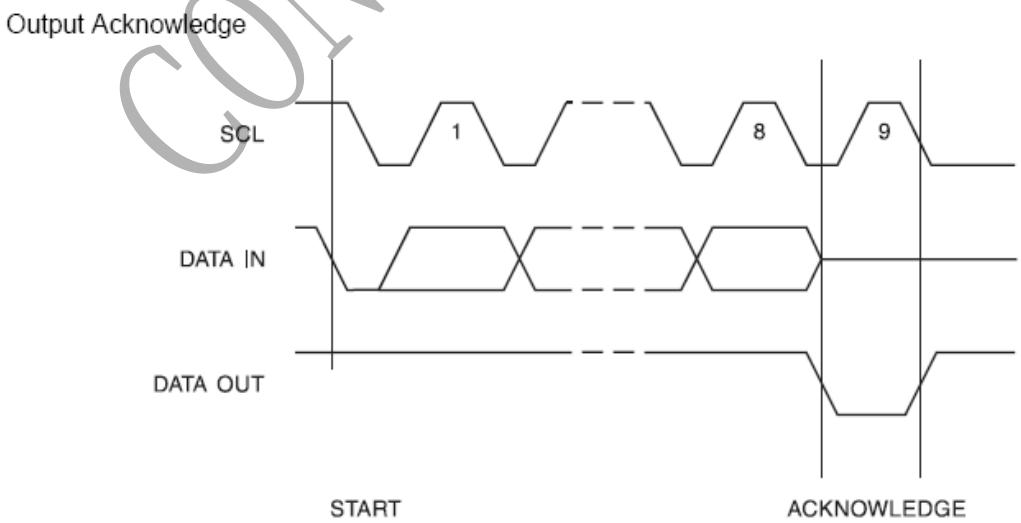
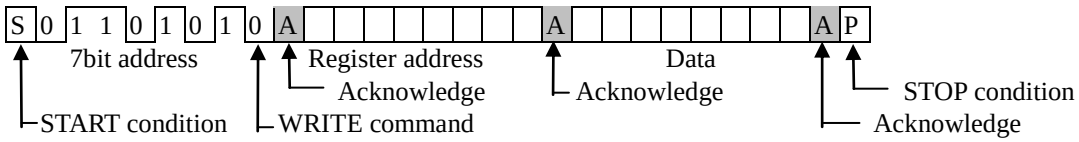


Figure 4: Acknowledge

2) BYTE WRITE:
The write operation is accomplished via a 3-byte sequence:
Serial address with write command

Register address
Register data

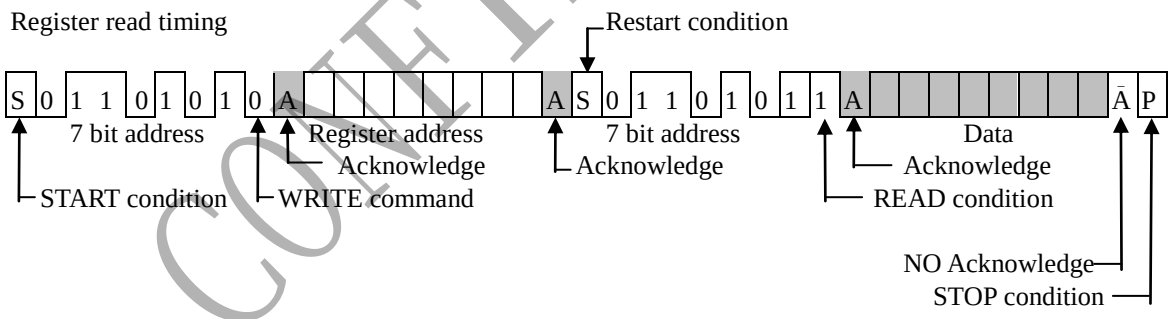
A write operation requires an 8-bit register address following the device address word and acknowledgment. Upon receipt of this address, the KT0937-D8 will again respond with a "0" and then clock in the 8-bit register data. Following receipt of the 8-bit register data, the KT0937-D8 will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition.



Note: The grey background is for the KT0937-D8 output. The white background is for the MCU output.

3) RANDOM READ:
The read operation is accomplished via a 4-byte sequence:
Serial address with write command
Register address
Serial address with read command
Register data

Once the device address and register address are clocked in and acknowledged by the KT0937-D8, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The KT0937-D8 acknowledges the device address and serially clocks out the register data. The microcontroller does not respond with a "0" but does generate a following stop condition.



Note: The grey background is for the KT0937-D8 output. The white background is for the MCU output.

5 The cautions of MCU interface configuration

The SDA pin and SCL pin of MCU must be configured into open-drain or open-collector mode.

When the SDA and SCL pin is configured in to push-pull mode, please DO NOT pull these two pins to high logic when ACK signal is arrived. The logic conflict will damage the ICs.

6 Audio common mode voltage

The value of the audio output common mode voltage is decided by the register of AUDV_DCLVL<2:0>, and this value will affect the maximum volume output by the chip. When the register of AUDV_DCLVL<2:0> is set to be 0, the common mode voltage is 0.85V and when it is set to be 7, the

common mode voltage is 1.6V. Normally, the common mode voltage should be set to be half of the power supply voltage. As the maximum swing of the audio output is $1.8V_{pp}$, the common voltage is suggested set to be 1.05V.

Registers	Address	Default Value	Access	Recommended Value
AUDV_DCLVL<2:0>	0x4E<2:0>	2	Read/Write	2（1.05v）

7 Configuration of KT0937-D8's volume

Those Registers of FM_GAIN<2:0>, MW_GAIN<3:0>, SW_VOLUME<3:0>, MW_VOLUME<3:0> , SW_VOLUME<3:0> and VOLUME<4:0> are related to the volume. In FM mode, the volume is controlled by the register of FM_GAIN<2:0>. MW_GAIN<3:0> together with MW_VOLUME<3:0> control the MW mode volume. SW_GAIN<3:0> together with MW_VOLUME<3:0> control the SW mode volume. VOLUME<4:0> controls the whole volume. The relationship of the control is shown as the Figure 5.

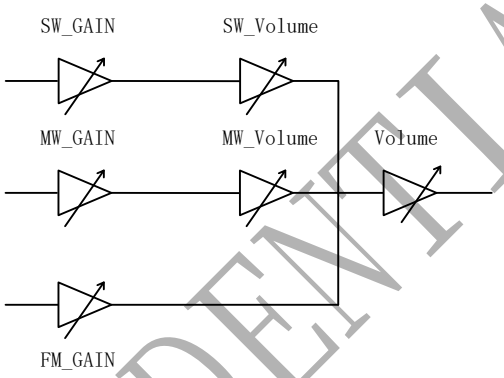


Figure 5: Volume control relationship

Registers	Address	Default Value	Access	Recommended Value
FM_GAIN<2:0>	0x2A<6:4>	4	Read/Write	4
MW_GAIN<3:0>	0x62<7:4>	4	Read/Write	4
MW_VOLUME<3:0>	0x69<3:0>	10	Read/Write	10
SW_GAIN<3:0>	0x38<3:0>	4	Read/Write	4
SW_VOLUME<3:0>	0x39<3:0>	10	Read/Write	10
VOLUME<4:0>	0x0F<4:0>	0x31	Read/Write	0x31

8 Mute

When the audio output of KT0937-D8 need to be muted, you should set the register of VOLUME <4:0> to be 0.

Registers	Address	Default Value	Access	Recommended Value
VOLUME<4:0>	0x0F<4:0>	31	Read/Write	0

9 De-pop configuration

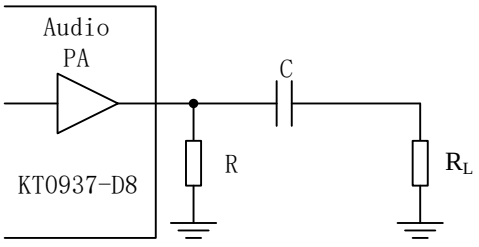


Figure 6: De-pop configuration

KT0937-D8 has the function of De-pop, which is used to suppress pop noise during power-on. Figure 6 is the schematic of the audio part. The first-order high-pass filter, whose Cutoff frequency is expressed $f = \frac{1}{2\pi R_L C}$, is made up of the capacitor C and the load R_L. The large value of AC-coupling capacitor C must be required when KT0937-D8 directly drive 32ohm headphone loads in order to get a better low-frequency characteristic. If it drives a audio power amplifier, a small value AC- coupling capacitor is okay.

The resister R in Figure 6 is used to discharge the AC-coupling capacitor C during power-down and de-pop circuit can work normally during power-on. The value of resistance R is too large lead to no time to discharge the capacitor C and then KT0937-D8 will have pop noise during power-on. The value of resistance R is too small lead to large leakage current. The leakage current is equal VCM / R. there will be 1.05mA leakage current when the VCM is 1.05V, and the value of register R is 1Kohm. Therefore 1Kohm-10Kohm resistor is recommended.

The charging time of AC-coupling capacitor C is decided by The DEPOP_TC<1:0>. The time can be configured from 250ms to 1s in 250ms step.

Even if KT0937-D8 audio output do not need any audio filter, there is also not any interfere frequency, the audio output signal don't affect AM reception.

Registers	Address	Default Value	Access	Recommended Value
DEPOP_TC<1:0>	0x4E<5:4>	3	Read/Write	3
AUDV_DCLVL<2:0>	0x4E<2:0>	2	Read/Write	2（1.05v）

10 How to enter standby mode

1) Setting the register STBYLDO_CALI_EN (0x10<6>) to 1.
2) Clearing the register STBYLDO_PD (0x76<1>) to 0.
3) KT0937-D8 works in Standby mode after setting STDBY (0x0E<5>) to 1.

Registers	Address	Default Value	Access	Recommended Value
STBYLDO_CALI_EN	0x10<6>	0	Read/Write	1
STBYLDO_PD	0x76<1>	0	Read/Write	0
STDBY	0x0E<5>	0	Read/Write	1

11 Waking up KT0937-D8

1) Clearing STDBY (0x0E<5>) to 0.
2) Delay 1ms.
3) Setting the register STBYLDO_PD (0x76<1>) to 1.
4) Reinitializing KT0937-D8.

Registers	Address	Default Value	Access	Recommended Value
STDBY	0x0E<5>	0	Read/Write	0
STBYLDO_PD	0x76<1>	0	Read/Write	1

12 Configuration for interrupt

Register TUNE_INT_EN is used to enable the interrupt. When TUNE_INT_EN=1, the change of CH pin voltage will lead to the interrupt signal of INT pin. When TUNE_INT_EN=0, whether CH pin voltage changes or not, the INT pin will not output the interrupt signal.

Register TUNE_INT_MODE is used to select the mode of interrupt. When TUNE_INT_MODE=1, KT0937 will output the pulse interrupt signal. When TUNE_INT_MODE=0, KT0937 will output the level interrupt signal.

Register TUNE_INT_PL is used to set the polarity of the interrupt signal while tuning. When TUNE_INT_PL=0, the output of interrupt is low level or negative pulse signal. When TUNE_INT_PL=1, the output of interrupt is high level or positive pulse signal.

There is no need to clear the interrupt in MCU when it shows the pulse signal, KT0937 can do it automatically. But if there is a low level signal showed, just set INT_PIN<1:0> in 2b'01 to clear the interrupt output. And as the case of high level signal, INT_PIN<1:0> should be set in 2b'10 to clear the interrupt output.

Registers	Address	Default Value	Access	Recommended Value
TUNE_INT_EN	0x22<7>	0	Read/Write	1
TUNE_INT_MODE	0x22<6>	0	Read/Write	-
TUNE_INT_PL	0x1F<7>	0	Read/Write	-
INT_PIN<1:0>	0x4F<1:0>	2	Read/Write	-

Table 1: Mode of Interrupt

Mode	TUNE_INT_MODE	TUNE_INT_PL	Clear Interrupt
Low Level	0	0	INT_PIN<1:0>=2b'01
High Level	0	1	INT_PIN<1:0>=2b'10
Negative Pulse	1	0	Auto
Positive Pulse	1	1	Auto

13 Setting register CH_ADC_WIN

The calculation methods of CH_ADC_WIN<12:0> are as followed:

CH_ADC_WIN<12:0> = (CHAN_NUM<11:0> + CH_GUARD<7:0>) * 2 **Equal 1**

Registers	Address	Default Value	Access	Recommended Value
CH_ADC_WIN<12:8>	0x74<4:0>	1	Read/Write	-
CH_ADC_WIN<7:0>	0x75<7:0>	0x14	Read/Write	-

14 Shut down the ADC of CH pin

CH_ADC_DIS is set to 1should shut down the ADC of CH pin.

Registers	Address	Default Value	Access	Recommended Value
CH_ADC_DIS	0x71<7>	0	Read/Write	1

15 Turn on the ADC of CH pin

After CH_ADC_DIS is cleared 0, CH_ADC_START is set to 1 should turn on the ADC of CH pin.
Note: CH_ADC_START register will be automatically cleared, after one clock cycle when it be set to 1.

Registers	Address	Default Value	Access	Recommended Value
CH_ADC_DIS	0x71<7>	0	Read/Write	0
CH_ADC_START	0x71<2>	0	Read/Write	1

FM Part

16 Setting FM band

Register AM_FM is used to set the working band, when CHANGE_BAND=1 means switching band is successful. After that the register CHANGE_BAND will be cleared into 0 by the device.

The steps of switching band are as followed:

1) Shut down the ADC of CH pin.
2) Set the band of range FM, which means register LOW_CHAN<14:0>, register CHAN_NUM<11:0> and register FM_HIGH_CHAN<11:0> must be configured.
3) Setting FM frequency step FM_SPACE<1:0>.
4) Setting CH_GUARD<7:0>.
5) Setting register CH_ADC_WIN<12:0>
6) Set register AM_FM=0 and register CHANGE_BAND=1, KT0937 can be working in FM channel mode.
7) Turn on the ADC of CH pin.
8) KT0937 will adjust to the channel that corresponding to CH potential device, after switching successful.

Registers	Address	Default Value	Access	Recommended Value
CH_ADC_DIS	0x71<7>	0	Read/Write	-
CH_ADC_START	0x71<2>	0	Read/Write	-
LOW_CHAN<14:8>	0x98<6:0>	0x01	Read/Write	-
LOW_CHAN<7:0>	0x99<7:0>	0xF8	Read/Write	-
CHAN_NUM<11:8>	0x9A<3:0>	0	Read/Write	-
CHAN_NUM<7:0>	0x9B<7:0>	0x86	Read/Write	-
FM_HIGH_CHAN<11:8>	0x88<3:0>	6	Read/Write	-
FM_HIGH_CHAN<7:0>	0x89<7:0>	0xB8	Read/Write	-
FM_SPACE<1:0>	0x18<5:4>	1	Read/Write	-
CH_GUARD<7:0>	0xA0<7:0>	0x17	Read/Write	-
CH_ADC_WIN<12:8>	0x74<4:0>	1	Read/Write	-
CH_ADC_WIN<7:0>	0x75<7:0>	0x14	Read/Write	-
AM_FM	0x88<6>	1	Read/Write	0
CHANGE_BAND	0x88<7>	0	Read/Write	1

17 Setting FM band range

In FM mode, you can set the start channel by register LOW_CHAN<14:0> and the register FM_HIGH_CHAN<11:0> can be set the end channel. The channel number can be set by register CHAN_NUM<11:0> and the frequency step can be set by register FM_SPACE<1:0>.

The calculation methods are as followed:

LOW_CHAN<14:0> = Channel start frequency (KHz) / 50 (KHz） Equal 2

FM_HIGH_CHAN<11:0> = Channel end frequency (KHz) / 50 (KHz） Equal 3

CHAN_NUM<11:0> = (Channel end frequency - Channel start frequency) / Frequency step (KHz) Equal 4

Example：set the channel band as 87.5-108MHz, and the frequency step 100KHz。

1) 87.5MHz / 50KHz = 1750, which is 0x06D6 in Hex, write 0xD6 into LOW_CHAN<7:0> while write 0x06 into LOW_CHAN<14:8>.
2) 108MHz / 50KHz = 2160, which is 0x870 in Hex, write 0x70 into FM_HIGH_CHAN<7:0> and write 0x08 into FM_HIGH_CHAN<11:8>.
3) (108MHz -87.5MHz) / 100KHz = 205, which is 0xCD in Hex, write 0xCD into CHAN_NUM<7:0> then write 0 into CHAN_NUM<11:8>.

Registers	Address	Default Value	Access	Recommended Value
LOW_CHAN<14:8>	0x98<6:0>	0x01	Read/Write	-
LOW_CHAN<7:0>	0x99<7:0>	0xF8	Read/Write	-
CHAN_NUM<11:8>	0x9A<3:0>	0	Read/Write	-
CHAN_NUM<7:0>	0x9B<7:0>	0x86	Read/Write	-
FM_HIGH_CHAN<11:8>	0x88<3:0>	6	Read/Write	-
FM_HIGH_CHAN<7:0>	0x89<7:0>	0xB8	Read/Write	-
FM_SPACE<1:0>	0x18<5:4>	1	Read/Write	-

18 De-emphasis time constant

The FM broadcasting pre-emphasis time constant has two different standards in the worldwide. The chip KT0937-D8 allows customers to define the de-emphasis time constant according to the situation. When the register DE is set to be 0, the DE-emphasis time constant is 75us and when DE is set to be 1, it is 50us.

Registers	Address	Default Value	Access	Recommended Value
DE	0x2B<3>	1	Read/Write	-

19 MONO and stereo demodulation

When the register MONO is set to be 0, the chip will chose demodulate mode by itself according to the current radio is stereo or a mono one. Listening to a weak stereo, the listening effect is poor, because the signal-to-noise ratio is very low. We can make the chip work at mono receiving mode, then the signal-to-noise ratio will be raised and the listen effect will become better. The chip has a built-in a force-mono circuit, it will enter mono demodulation mode if the register MONO is set to be 1.

Registers	Address	Default Value	Access	Recommended Value
MONO	0x2B<7>	0	Read/Write	0

20 Stereo indication

KT0937-D8 has the function of stereo indication, which not only indicates whether the current channel is a stereo station, but also indicates whether the current channel demodulates as the stereo station.
The chip identifies the stereo station as the following steps.

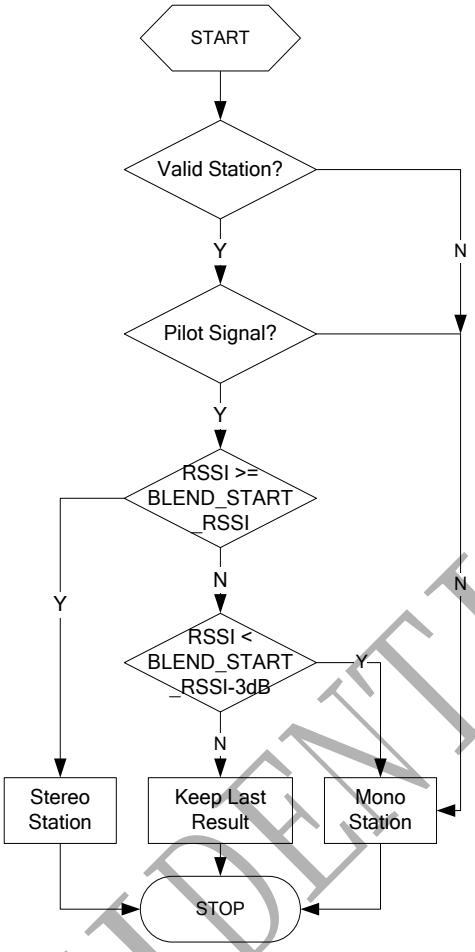


Figure 7: Flow chart of stereo station judgment

Every several milliseconds, KT0937-D8 decides whether the current channel is a stereo station, which depends on the following three statements, whether the current channel is a valid station, whether the pilot signal is detected, and the RSSI. If the current channel is an invalid station, or the pilot signal is undetected, the current channel is considered as a mono station. Otherwise, the decision is determined by the RSSI. The current channel is considered as a stereo station if the RSSI is greater than or equals the value of the register BLEND_START_RSSI<3:0>, as a mono station if the RSSI is less than the value of the register BLEND_START_RSSI<3:0> minus 3dB. If the RSSI is less than the value of the register BLEND_START_RSSI<3:0>, and is greater than the value of the register BLEND_START_RSSI<3:0> minus 3dB, the chip keeps the determination of the last time.

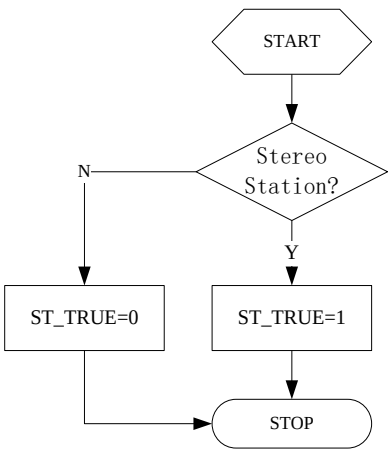


Figure 8: Flow chart ST_TRUE

Users could get the determination result of whether the current channel is a stereo station, by reading the values of register ST_TRUE. When the value of register ST_TRUE is 1, the current channel is a stereo station; otherwise, it is a mono station.

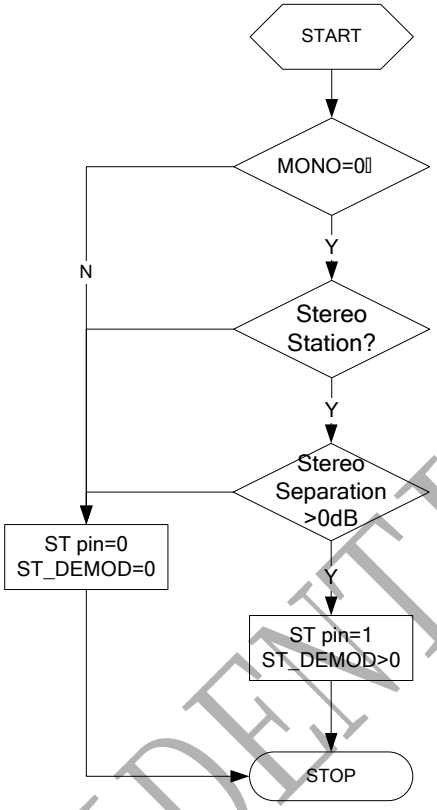


Figure 9: Stereo indication

KT0937-D8 will demodulate the received signal as a mono station if one of the following statements is true, the current channel is determined as a mono station, the register of MONO is set to 1 by user, or the value of stereo separation calculated by BLEND function is 0dB. Meanwhile, the ST pin outputs 0 and the read-only register ST_DEMOD<7:0> equals 0. Otherwise, the signal will be demodulated in stereo mode, at the same time, the ST pin outputs 1, the read-only register ST_DEMOD<7:0> will be greater than 0.

Registers	Address	Default Value	Access	Recommended Value
BLEND_START_RSSI<3:0>	0x2C<7:4>	5	Read/Write	5
ST_TRUE	0xDE<0>	0	Read Only	-
ST_DEMOD<7:0>	0x1C<7:0>	0	Read Only	-
MONO	0x2B<7>	0	Read/Write	0

21 FM frequency difference

Due to the accuracy of the crystal, there is a difference of the receiving frequency of KT0937-D8. If the accuracy of the crystal is 50ppm, the difference is about 5 KHz when receive the 100MHz signal. Frequency difference correction function can be turned off when the register FM_AFCD set to 1. The register FM_TH_AFC<2:0> decides the maximum range of correctable. FM frequency difference is calculated as follows:

FM frequency difference = | 2 * AFC_AAF<7:0> - FM_CARRIER_OFST<7:0> | * 1KHz

KT0937-D8 can detect the difference between the set frequency and the actual radio frequency, KT0937-D8 will correct when difference is less than FM_TH_AFC<2:0>threshold.

AFC_AAF<7:0> register indicates the current AFC correction amount, the unit is 2048Hz.

For FM mode, the register FM_CARRIER_OFST<7:0> indicates that the difference between the corrected frequency and the actual radio frequency, the unit is 1024Hz.

The Examples of FM frequency difference: the actual radio frequency is 100.000MHz when frequency receiver is 100.00512MHz. Frequency correction process is shown in 错误！书签自引用无效。. The register AFC_AA<7:0> is 1 (2.048KHz), the register FM_CARRIER_OFST<7:0> is -3 (-3.072KHz). FM frequency difference = 1 * 2.048 - (-3 * 1.024) = 5.12KHz.

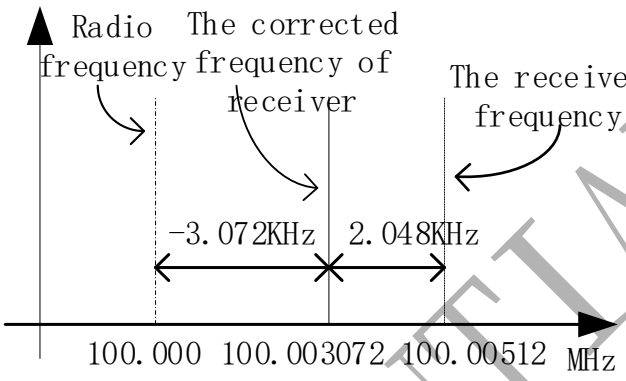


Figure 10: FM frequency difference

Registers	Address	Default Value	Access	Recommended Value
FM_AFCD	0x3E<6>	0	Read/Write	0
FM_TH_AFC<2:0>	0x3E<2:0>	3	Read/Write	7
AFC_AAF<7:0>	0x79<7:0>	0	Read Only	-
FM_CARRIER_OFST<7:0>	0xE9<7:0>	0	Read Only	-

22 Reading the current frequency in FM mode

You can get the current frequency by reading the value of the register RDCHAN<11:0>. In FM mode, the unit is 50KHz. The calculate method is as follows:

The current frequency (KHz) = RDCHAN<11:0> * 50.

Registers	Address	Default Value	Access
RDCHAN<11:8>	0xE4<3:0>	0	Read Only
RDCHAN<7:0>	0xE5<7:0>	0	Read Only

23 RF signal strength indicator in FM mode

FM_RSSI<6:0> register is used to indicate the value of the RF signal strength of the current station in FM mode. The range of register value is 0-0x78. The register value 0 indicates -110dBm. 0x78 means 10dBm signal.

Calculated as follows:
FM RF signal strength (dBm) = FM_RSSI<6:0>- 110
FM RF signal strength (dBuV) = FM_RSSI<6:0> - 3
FM RF signal strength (dBuVEMF) = FM_RSSI<6:0> + 3

Registers	Address	Default Value	Access
FM_RSSI<6:0>	0xE6<6:0>	0	Read Only

24 SNR meter in FM mode

In FM mode, by reading FM_SNR<6:0> register value can be obtained SNR of the current station. SNR is the worst when the value is 0. SNR is the best when the value is 0x7F.

Registers	Address	Default Value	Access
FM_SNR<6:0>	0xE2<6:0>	0	Read Only

25 FM valid station

In FM mode, valid tune module is used to judge whether the current receive channel is valid tune. There are three judgment conditions:

- ✧ The condition RSSI should meet.
  In FM mode, the RSSI value can be read from register FM_RSSI<6:0>, the RSSI threshold is depend on register FM_TUN_RSSI_HITH<2:0> and FM_TUN_RSSI_LOWTH<2:0>. When the RSSI value is bigger than the high threshold FM_TUN_RSSI_HITH<2:0>, it meets the condition. When the RSSI value is smaller than the low threshold FM_TUN_RSSI_LOWTH<2:0>, it does not meet the condition. When the RSSI value is between the high threshold FM_TUN_RSSI_HITH<2:0> and the low threshold FM_TUN_RSSI_LOWTH<2:0>, whether it meets the condition according to the last judgment, and it is a hysteretic interval.

- ✧ The condition SNR should meet.
  In FM mode, the SNR value can be read from register FM_SNR<5:0>, the SNR threshold is depend on register FM_TUN_SNR_HITH<2:0> and FM_TUN_SNR_LOWTH<2:0>. When the SNR value is bigger than the high threshold FM_TUN_SNR_HITH<2:0>, it meets the condition. When the SNR value is smaller than the low threshold FM_TUN_SNR_LOWTH<2:0>, it does not meet the condition. When the SNR value is between the high threshold FM_TUN_SNR_HITH<2:0> and the low threshold FM_TUN_SNR_LOWTH<2:0>, whether it meets the condition according to the last judgment, and it is a hysteretic interval.

- ✧ The condition uncorrected frequency difference should meet.
  In FM mode, the uncorrected frequency difference can be read from register FM_CARRIER_OFST<7:0>, the unit is 1024Hz. When uncorrected frequency difference is bigger than 21KHz, it does not meet the condition. When uncorrected frequency difference is smaller than 12KHz, it meets the condition. When the uncorrected frequency difference is between 12KHz and 21KHz, whether it meets the condition according to the last judgment, that is it is a hysteretic interval.
  If the three conditions are all met, it is a valid tune. Otherwise it is an invalid tune. The judgment flow is as flowing:

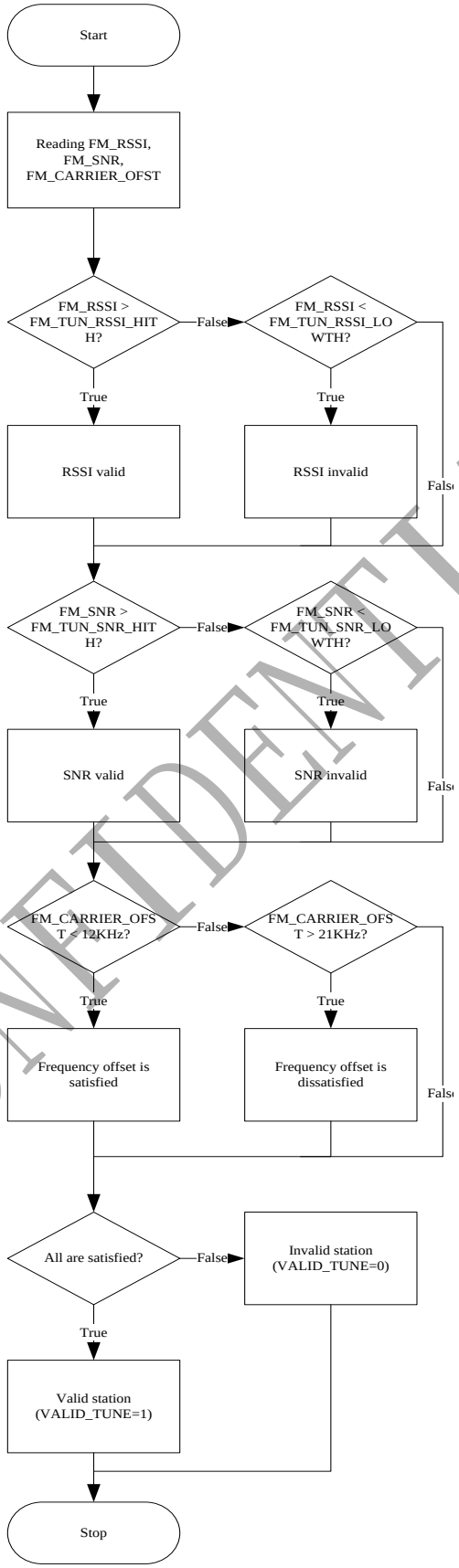


Figure 11: Flow chart of FM valid tune judgment

Registers	Address	Default Value	Access	Recommended Value
FM_TUN_RSSI_HITH<2:0>	0x80<6:4>	5	Read/Write	5
FM_TUN_RSSI_LOWTH<2:0>	0x80<2:0>	3	Read/Write	3
FM_TUN_SNR_HITH<2:0>	0x7F<6:4>	5	Read/Write	5
FM_TUN_SNR_LOWTH<2:0>	0x7F<2:0>	5	Read/Write	5
FM_RSSI<6:0>	0xE6<6:0>	0	Read only	-
FM_SNR<5:0>	0xE2<5:0>	0	Read only	-
FM_CARRIER_OFST<7:0>	0xE9<7:0>	0	Read only	-
VALID_TUNE	0xDE<2>	0	Read only	-

26 Softmute setting of FM mode

When the quality of the input RF signal deteriorates, the output audio quality cannot be guaranteed. Sometimes, there could be harsh noise or broken sound. In such cases, users would be less annoyed if the audio volume could be reduced. KT0937-D8 offers the function of SOFTMUTE, which automatically decreases the audio volume when the quality of the input signal deteriorates, to improve the experience of the users, as in Figure 12.

The function of SOFTMUTE is enabled by setting the register FM_DSMUTE to 0. The attenuation of the volume is controlled by the RSSI, the SNR, and the register FM_SMUTE_MIN_GAIN<2:0>. KT0937-D8 calculates two values of volume attenuation, which are determined by RSSI and SNR separately. Then the two values are added in dB. Finally, the sum is saturated by the value set by the register FM_SMUTE_MIN_GAIN<2:0>, which will determine the actual volume attenuation, as shown in the point 11 of Figure 12.

The value of volume attenuation determined by SNR is calculated as follows. When the SNR of the input RF signal is less than the value set by the register FM_SMUTE_START_SNR<5:0>, the volume attenuation is enabled, as shown in the point 1 of Figure 12. While, the value set by the register FM_SMUTE_SLOPE_SNR<2:0> represents the slope of the attenuation. In this case, the attenuation should not be greater than 12dB, as in the point 2 of Figure 12.

The value of volume attenuation determined by RSSI is calculated as follows. When the RSSI of the input RF signal is less than the value set by the register FM_SMUTE_START_RSSI<2:0>, the volume attenuation is enabled, as shown in the point 5 of Figure 12. While, the value set by the register FM_SMUTE_SLOPE_RSSI<2:0> represents the slope of the attenuation. In this case, the attenuation should not be greater than 21dB, as in the point 6 of Figure 12.

The calculated volume attenuation by SOFTMUTE function could be obtained by reading register SMUTE_GAIN<7:0>, where the number in dB can be computed by the following equation: $20\log\frac{\text{SMUTE\_GAIN<7:0>}}{128}$. By writing the register SMUTE_GAIN<7:0> directly, user can also control the volume attenuation by MCU rather than the built-in SOFTMUTE function, after the SMUTE_GAIN_CTRL_EN is set to 1.

Setting the register SMUTE_FILTER_EN to 1 enables the filter of SOFTMUTE, to reduce the noise when the volume attenuation changes.

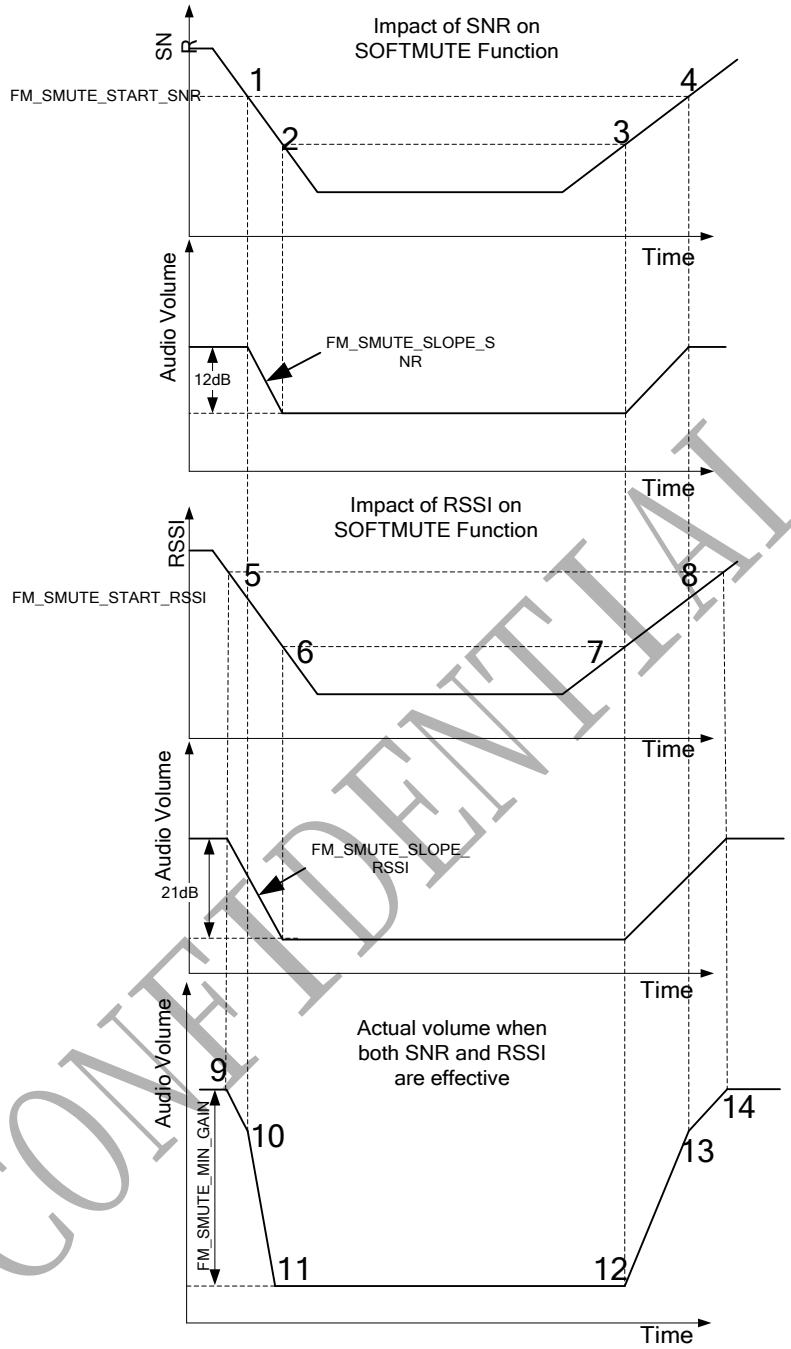


Figure 12: Illustration of SOFTMUTE in FM mode

Registers	Address	Default Value	Access	Recommended Value
FM_DSMUTE	0x1A<7>	0	Read/Write	0
FM_SMUTE_START_RSSI<2:0>	0x1F<6:4>	5	Read/Write	5
FM_SMUTE_SLOPE_RSSI<2:0>	0x1F<2:0>	3	Read/Write	3
FM_SMUTE_START_SNR<5:0>	0x22<5:0>	0x15	Read/Write	0x15
FM_SMUTE_SLOPE_SNR<2:0>	0x21<2:0>	2	Read/Write	4
SMUTE_GAIN_CTRL_EN	0x87<5>	0	Read/Write	0
SMUTE_GAIN<7:0>	0xE3<7:0>	0x00	Read/Write	-
SMUTE_FIL_EN	0x2F<1>	0	Read/Write	1
FM_SMUTE_MIN_GAIN<2:0>	0x19<4:2>	4	Read/Write	3

27 BLEND in FM mode

In FM mode, when the receiving signal is weak, the SNR of the demodulated signal in stereo mode is lower than that in mono mode, more noise will be heard by the end-users. To solve this problem, BLEND technique is adopted in KT0937-D8.

With the RF signal quality of a stereo station improving, the separation of the left audio channel and the right one gradually increases, according to the specified criteria. Once the RF signal is strong enough, the two channels are completely separated, and the separation reaches the maximum. This procedure is called "gradually separation of the stereo demodulation", which provides a smooth hearing experience with a constant noise level when the quality of RF signals is varying, as shown in Figure 13.

To enable BLEND function, the register of DBLEND should be set to 0. There are three BLEND modes provided by KT0937-D8, which are determined by register BLEND_MOD and BLEND_COMBO_MODE, described as follows:

When BLEND_MOD=0 and BLEND_COMBO_MODE=0, the RSSI is adopted as the criteria of adjusting stereo separation in BLEND function. If the RSSI is less than the value set by register BLEND_START_RSSI<3:0>, KT0937-D8 demodulates in mono mode, which means that the stereo separation is 0dB. When the RSSI is greater than the value set by register BLEND_STOP_RSSI<3:0>, KT0937-D8 demodulates in fully stereo mode, which means the stereo separation reaches maximum. If the RSSI is between the above two thresholds, the function of "gradually separation" takes effect. The stereo separation would be adjusted according to the RSSI of the receiving signal.

When BLEND_MOD=1 and BLEND_COMBO_MODE=0, the SNR is adopted as the criteria of adjusting stereo separation in BLEND function. If the SNR is less than the value set by register BLEND_START_SNR<5:0>, KT0937-D8 demodulates in mono mode, which means the stereo separation is 0dB. When the SNR is greater than the value set by register BLEND_STOP_SNR<5:0>, KT0937-D8 demodulates in fully stereo mode, which means that the stereo separation reaches maximum. If the SNR is between the above two thresholds, the function of "gradually separation" takes effect, and the stereo separation is adjusted according to the SNR of the receiving signal.

When BLEND_COMBO_MODE=1, another criteria, which mixes the value of RSSI and SNR, is adopted in BLEND function. If either of RSSI and SNR is less than the value set by BLEND_START_COMBO<2:0>, KT0937-D8 demodulates in mono mode, which means the stereo separation is 0dB. When both of RSSI and SNR exceed the values set by BLEND_START_COMBO<2:0> plus 21dB, KT0937-D8 demodulates in fully stereo mode, which means that the stereo separation reaches maximum. If the above two statements are not true, the function of "gradually separation" takes effect, and the stereo separation is adjusted according to one of criteria in RSSI and SNR, which implies the quality of RF signal is worse.

Besides, KT0937-D8 offers another mode, called "immediately separation", which means that the separation of the left audio channel and the right one will be changed from 0dB to the maximum, once the quality of RF signal exceeds the certain threshold of the adopted criteria, as shown in Figure 14. The experience of the "immediately separation" users is very different from that of "gradually separation". The "immediately separation" can be configured as follows:

When BLEND_MOD=0 and BLEND_COMBO_MODE=0, the register BLEND_START_RSSI<3:0> and BLEND_STOP_RSSI<3:0> should be set to the same value. When RSSI is less than the set value minus 3dB, mono demodulation is enabled. When RSSI is greater than the set value, fully stereo demodulation is enabled. If neither of the above two statements is satisfied, the demodulation mode will be kept as the last time when RSSI is updated.

When BLEND_MOD=1 and BLEND_COMBO_MODE=0, the register BLEND_START_SNR<5:0> and BLEND_STOP_SNR<5:0> should be set to the same value. When SNR is less than the set value minus 3dB, mono demodulation is enabled. When SNR is greater than the set value, fully stereo demodulation is

enabled. If neither of the above two statements is satisfied, the demodulation mode will be kept as the last time when SNR is updated.

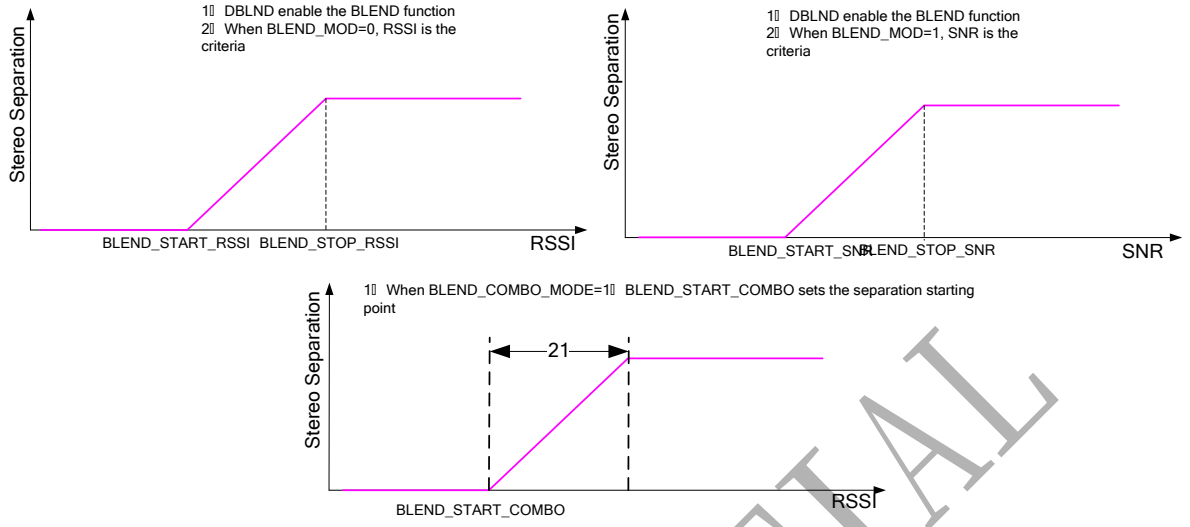


Figure 13: Illustration of Gradually Separation

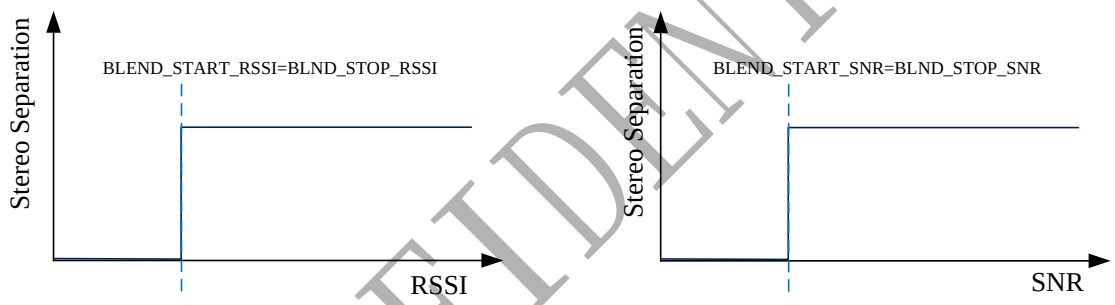


Figure 14: Illustration of Immediately Separation

Registers	Address	Default Value	Access	Recommended Value
DBLEND	0x2B<0>	0	Read/Write	0
BLEND_MOD	0x29<4>	0	Read/Write	0
BLEND_START_RSSI<3:0>	0x2C<7:4>	5	Read/Write	5
BLEND_STOP_RSSI<3:0>	0x2C<3:0>	15	Read/Write	15
BLEND_START_SNR<5:0>	0x34<5:0>	0	Read/Write	0x3F
BLEND_STOP_SNR<5:0>	0x35<5:0>	0	Read/Write	0x3F
BLEND_COMBO_MODE	0x2F<4>	0	Read/Write	1
BLEND_START_COMBO<2:0>	0x7E<6:4>	0	Read/Write	2

28 AM suppression

When the AM_SUP_ENHANCE register is enabled, the AM suppression can be enhanced in FM mode.

Registers	Address	Default Value	Access	Recommended Value
AM_SUP_ENHANCE	0x2F<2>	0	Read/Write	1

MW Part

29 Setting MW band

Register AM_FM is used to set the working band, when CHANGE_BAND=1 means switching band is successful. After that the register CHANGE_BAND will be cleaned into 0 by the device.

The steps of switching band are as followed:

1) Shut down the ADC of CH pin.
2) Set the band range of MW, which means register LOW_CHAN<14:0>, register CHAN_NUM<11:0> and register AM_HIGH_CHAN<14:0> must be configured.
3) Setting FM frequency step MW_SPACE<1:0>.
4) Setting CH_GUARD<7:0>.
5) Setting register CH_ADC_WIN<12:0>
6) Set register AM_FM=1 and register CHANGE_BAND=1, KT0937 can be working in MW channel mode.
7) Turn on the ADC of CH pin.
8) KT0937 will adjust to the channel that corresponding to CH potential device, after switching successful.

Registers	Address	Default Value	Access	Recommended Value
CH_ADC_DIS	0x71<7>	0	Read/Write	-
CH_ADC_START	0x71<2>	0	Read/Write	-
LOW_CHAN<14:8>	0x98<6:0>	0x01	Read/Write	-
LOW_CHAN<7:0>	0x99<7:0>	0xF8	Read/Write	-
CHAN_NUM<11:8>	0x9A<3:0>	0	Read/Write	-
CHAN_NUM<7:0>	0x9B<7:0>	0x86	Read/Write	-
AM_HIGH_CHAN<14:8>	0x8C<6:0>	1	Read/Write	-
AM_HIGH_CHAN<7:0>	0x8D<7:0>	0xF8	Read/Write	-
MW_SPACE<1:0>	0x18<1:0>	1	Read/Write	0
CH_GUARD<7:0>	0xA0<7:0>	0x17	Read/Write	-
CH_ADC_WIN<12:8>	0x74<4:0>	1	Read/Write	-
CH_ADC_WIN<7:0>	0x75<7:0>	0x14	Read/Write	-
AM_FM	0x88<6>	1	Read/Write	1
CHANGE_BAND	0x88<7>	0	Read/Write	1

30 Setting MW band range

In MW mode, you can set the start channel by register LOW_CHAN<14:0> and the register AM_HIGH_CHAN<14:0> can be set the end channel. The channel number can be set by register CHAN_NUM<11:0> and the frequency step can be set by register MW_SPACE<1:0>.

The calculation methods are as followed:

LOW_CHAN<14:0> = Channel start frequency (KHz) / 1 (KHz) **Equal 5**

AM_HIGH_CHAN<14:0> = Channel end frequency (KHz) / 1 (KHz) **Equal 6**

CHAN_NUM<11:0> = (Channel end frequency - Channel start frequency) / Frequency step (KHz) **Equal 7**

Example：set the channel band as 522-1620KHz, and the frequency step 1KHz。

1) 522KHz / 1KHz = 522, which is 0x020A in Hex, write0x0A into LOW_CHAN<7:0> while write 0x02 into LOW_CHAN<14:8>.
2) 1620KHz / 1KHz = 1620, which is 0x654 in Hex, write0x54 into AM_HIGH_CHAN<7:0> and write 0x06 into AM_HIGH_CHAN<14:8>.
3) (1620KHz -522KHz) / 1KHz = 1098, which is 0x44A in Hex, write 0x4A into CHAN_NUM<7:0> then write 0x04 into CHAN_NUM<11:8>.

Registers	Address	Default Value	Access	Recommended Value
LOW_CHAN<14:8>	0x98<6:0>	0x01	Read/Write	-
LOW_CHAN<7:0>	0x99<7:0>	0xF8	Read/Write	-
CHAN_NUM<11:8>	0x9A<3:0>	0	Read/Write	-
CHAN_NUM<7:0>	0x9B<7:0>	0x86	Read/Write	-
AM_HIGH_CHAN<14:8>	0x8C<3:0>	1	Read/Write	-
AM_HIGH_CHAN<7:0>	0x8D<7:0>	0xF8	Read/Write	-
MW_SPACE<1:0>	0x18<1:0>	1	Read/Write	0

31 MW frequency difference

Due to the accuracy of the crystal, there is a difference of the receiving frequency of KT0937-D8. If the accuracy of the crystal is 50ppm, the difference is about 50 Hz when receive the 1MHz signal. Frequency difference correction function can be turned off when the register MW_AFCD set to 1. The register MW_TH_AFC<2:0> decides the maximum range of correctable. MW frequency difference is calculated as follows:

MW frequency difference = | AFC_AAF<7:0> - AM_CARRIER_OFST<7:0> | * 128Hz

KT0937-D8 can detect the difference between the set frequency and the actual radio frequency, KT0937-D8 will correct when difference is less than MW_TH_AFC<2:0>threshold.

AFC_AAF<7:0> register indicates the current AFC correction amount, the unit is 128Hz.

The register AM_CARRIER_OFST<7:0> indicates that the difference between the corrected frequency and the actual radio frequency, the unit is 128Hz.

The Examples of MW frequency difference: the actual radio frequency is 1000KHz when frequency receiver is 1000.640KHz. Frequency correction process is shown in Figure 15. The register AFC_AAF<7:0> is 2 (256 Hz), the register AM_CARRIER_OFST<7:0> is -3 (-384 Hz). AM frequency difference = 2 * 128 - (-3 * 128) = 640Hz.

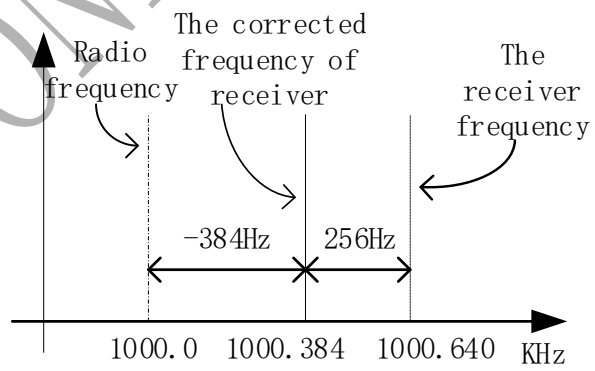


Figure 15: MW frequency difference

Registers	Address	Default Value	Access	Recommended Value
MW_AFCD	0x3F<6>	0	Read/Write	0
MW_TH_AFC<2:0>	0x3F<2:0>	0	Read/Write	3
AFC_AAF<7:0>	0x79<7:0>	0	Read Only	-
AM_CARRIER_OFST<7:0>	0xE8<7:0>	0	Read Only	-

32 Reading the current frequency in MW mode

You can get the current frequency by reading the value of the register RDCHAN<11:0>. In MW mode, the unit is 1KHz. The calculate method is as follows:

The current frequency (KHz) = RDCHAN<11:0>.

Registers	Address	Default Value	Access
RDCHAN<11:8>	0xE4<3:0>	0	Read Only
RDCHAN<7:0>	0xE5<7:0>	0	Read Only

33 RF signal strength indicator in MW mode

AM_RSSI<6:0> register is used to indicate the value of the RF signal strength of the current station in MW mode. The range of register value is 0-0x78. The register value 0 indicates -110dBm. 0x78 means 10dBm signal.

Calculated as follows:
MW RF signal strength (dBm) = AM_RSSI<6:0> - 110
MW RF signal strength (dBuV) = AM_RSSI<6:0> - 3
MW RF signal strength (dBuVEMF) = AM_RSSI<6:0> + 3

Registers	Address	Default Value	Access
AM_RSSI<6:0>	0xEA<6:0>	0	Read Only

34 SNR meter in MW mode

In MW mode, by reading AM_SNR_MODE1<6:0>register value can be obtained SNR of the current station. SNR is the worst when the value is 0. SNR is the best when the value is 0x7F.

FLT_SEL<2:0> register configuration will affect the SNR. The SNR will be higher when the bandwidth is narrower.

Registers	Address	Default Value	Access
AM_SNR_MODE1<6:0>	0xEC<6:0>	0	Read Only

35 MW valid station

In MW mode, valid tune module is used to judge whether the current receive channel is valid tune. There are three judgment conditions:

- ✧ The condition RSSI should meet.
  In MW mode, the RSSI value can be read from register AM_RSSI<6:0>, the RSSI threshold is depend on register MW_TUN_RSSI_HITH<6:0> and MW_TUN_RSSI_LOWTH<6:0>. When the RSSI value is bigger than the high threshold MW_TUN_RSSI_HITH<6:0>, it meets the condition. When the RSSI value is smaller than the low threshold MW_TUN_RSSI_LOWTH<6:0>, it does not meet the condition. When the RSSI value is between the high threshold MW_TUN_RSSI_HITH<6:0> and the low threshold MW_TUN_RSSI_LOWTH<6:0>, whether it meets the condition according to the last judgment, and it is a hysteretic interval.

- ✧ The condition SNR should meet.
  In MW mode, the SNR value can be read from register AM_SNR_MODE1<6:0>, the SNR threshold is depend on register MW_TUN_SNR_HITH<6:0> and MW_TUN_SNR_LOWTH<6:0>. When the SNR value is bigger than the high threshold MW_TUN_SNR_HITH<6:0>, it meets the condition. When the SNR value is smaller than the low threshold MW_TUN_SNR_LOWTH<6:0>, it does not

meet the condition. When the SNR value is between the high threshold MW_TUN_SNR_HITH<6:0> and the low threshold MW_TUN_SNR_LOWTH<6:0>, whether it meets the condition according to the last judgment, and it is a hysteretic interval.

✧ The condition uncorrected frequency difference should meet.
In MW mode, the uncorrected frequency difference can be read from register AM_CARRIER_OFST<7:0>, the unit is 128Hz. When uncorrected frequency difference is bigger than 3KHz, it does not meet the condition. When uncorrected frequency difference is smaller than 2KHz, it meets the condition. When the uncorrected frequency difference is between 2KHz and 3Khz, whether it meets the condition according to the last judgment, that is it is a hysteretic interval.

If the three conditions are all met, it is a valid tune VALID_TUNE=1. Otherwise it is an invalid tune VALID_TUNE=0. The judgment flow is as flowing:

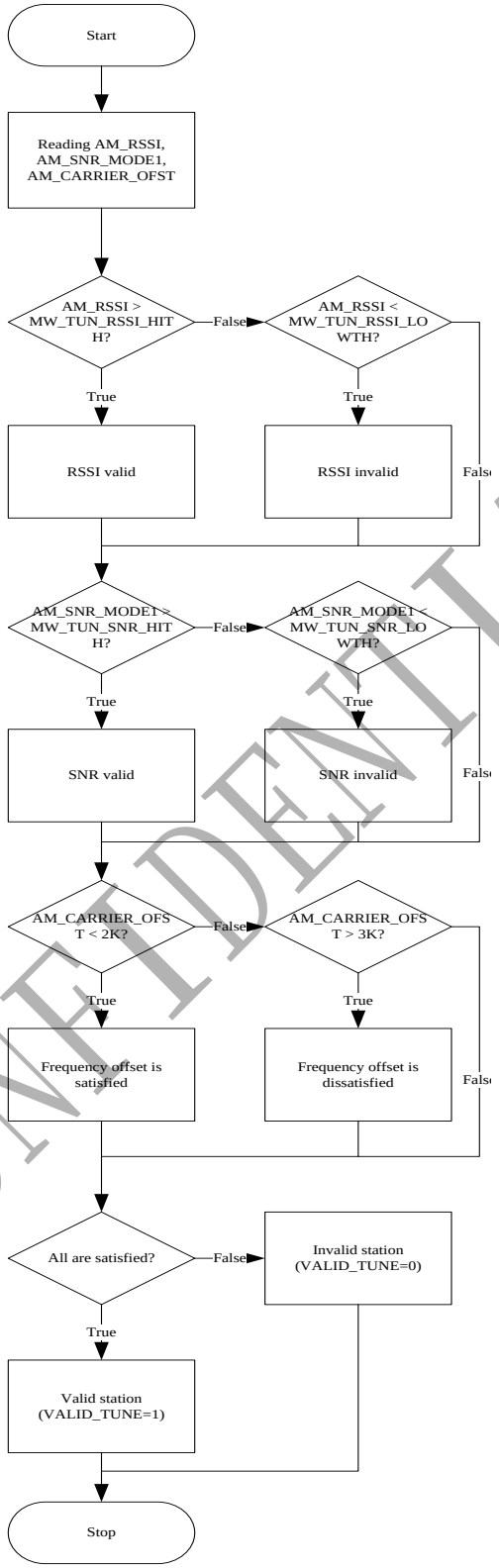


Figure 16: Flow chart of MW valid tune judgment

Registers	Address	Default Value	Access	Recommended Value
MW_TUN_RSSI_HITH<6:0>	0x83<6:0>	0x24	Read/Write	0x24
MW_TUN_RSSI_LOWTH<6:0>	0x84<6:0>	0x1F	Read/Write	0x1F
MW_TUN_SNR_HITH<6:0>	0x81<6:0>	0x3A	Read/Write	0x3A
MW_TUN_SNR_LOWTH<6:0>	0x82<6:0>	0x35	Read/Write	0x35
AM_RSSI<6:0>	0xEA<6:0>	0	Read only	-
AM_SNR_MODE1<6:0>	0xEC<6:0>	0	Read only	-
AM_CARRIER_OFST<7:0>	0xE8<7:0>	0	Read only	-
VALID_TUNE	0xDE<2>	0	Read only	-

36 Softmute setting of MW mode

When the quality of the input RF signal deteriorates, the output audio quality cannot be guaranteed. Sometimes, there could be harsh noise or broken sound. In such cases, users would be less annoyed if the audio volume could be reduced. KT0937-D8 offers the function of SOFTMUTE, which automatically decreases the audio volume when the quality of the input signal deteriorates, to improve the experience of the users, as in Figure 17.

The function of SOFTMUTE is enabled by setting the register MW_DSMUTE to 0. The attenuation of the volume is controlled by the RSSI, the SNR, and the register MW_SMUTE_MIN_GAIN<2:0>. KT0937-D8 calculates two values of volume attenuation, which are determined by RSSI and SNR separately. Then the two values are added in dB. Finally, the sum is saturated by the value set by the register MW_SMUTE_MIN_GAIN<2:0>, which will determine the actual volume attenuation, as shown in the point 11 of Figure 17.

The value of volume attenuation determined by SNR is calculated as follows. When the SNR of the input RF signal is less than the value set by the register MW_SMUTE_START_SNR<6:0>, the volume attenuation is enabled, as shown in the point 1 of Figure 17. While, the value set by the register MW_SMUTE_SLOPE_SNR<2:0> represents the slope of the attenuation. In this case, the attenuation should not be greater than 12dB, as in the point 2 of Figure 17.

The value of volume attenuation determined by RSSI is calculated as follows. When the RSSI of the input RF signal is less than the value set by the register MW_SMUTE_START_RSSI<6:0>, the volume attenuation is enabled, as shown in the point 5 of Figure 17. While, the value set by the register MW_SMUTE_SLOPE_RSSI<2:0> represents the slope of the attenuation. In this case, the attenuation should not be greater than 21dB, as in the point 6 of Figure 17.

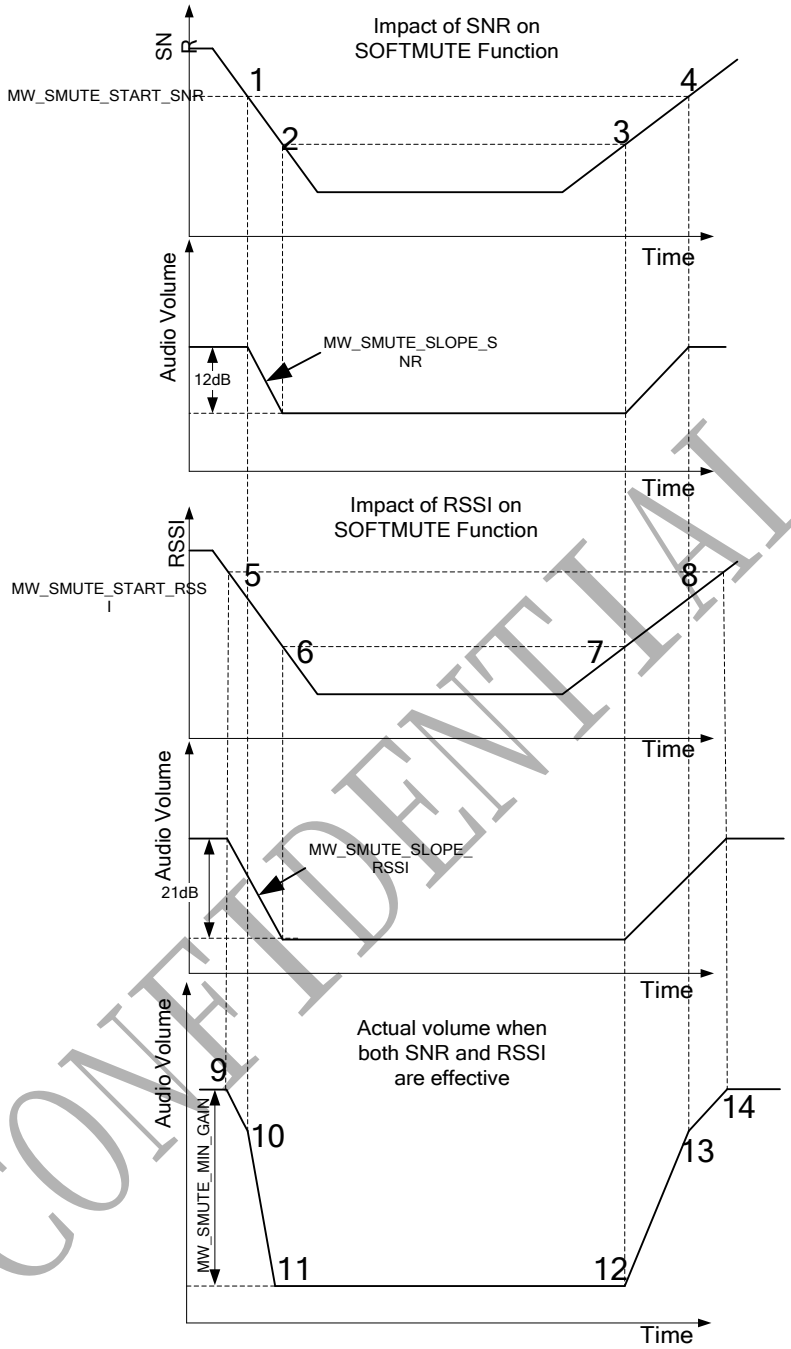


Figure 17: Illustration of SOFTMUTE in MW mode

Registers	Address	Default Value	Access	Recommended Value
MW_DSMUTE	0x1A<6>	0	Read/Write	0
MW_SMUTE_START_RSSI<6:0>	0x1D<6:0>	0x17	Read/Write	0x17
MW_SMUTE_SLOPE_RSSI<2:0>	0x1E<2:0>	4	Read/Write	4
MW_SMUTE_START_SNR<6:0>	0x20<6:0>	0x30	Read/Write	0x30
MW_SMUTE_SLOPE_SNR<2:0>	0x21<6:4>	0	Read/Write	0
MW_SMUTE_MIN_GAIN<2:0>	0x19<7:5>	1	Read/Write	1

37 Antenna tuning

If the ANT_CALI_SW_BAND register is enabled, the chip will implement antenna tuning operation when switching to MW band.

Registers	Address	Default Value	Access	Recommended Value
ANT_CALI_SWITCH_BAND	0x2F<5>	0	Read/Write	1

38 MW antenna tuning capacitor value monitor

Register CAP<13:0> means the value of antenna tuning capacitor in MW mode. The value of the antenna tuning capacitor is minimum, when the register CAP is equal to 0. The value of the antenna tuning capacitor is maximum, when the register CAP if equal to 0x3FFF. The antenna tuning capacitor makes up resonance loop with the off-chip ferrite antenna. The antenna tuning capacitor value can be used to determine whether the ferrite antenna inductance is appropriate, and whether it cannot be tuning.

Registers	Address	Default Value	Access
CAP<13:8>	0x56<5:0>	0	Read Only
CAP<7:0>	0x57<7:0>	0	Read Only

39 MW IF filter bandwidth configuration

The FLT_SEL<2:0> register is used to adjust the bandwidth of intermediate frequency filter in MW receiver. The narrow bandwidth of filter helps to suppress adjacent channel interference and reduce noise. It can improve audio SNR when RF signal is weak or there are some strong interference signals. If the narrow bandwidth of filter is used, the high frequency component of audio signal will be attenuate and there is a poor frequency response.

User can configure the FLT_SEL<2:0> register to obtain the different bandwidth of intermediate frequency filter, such as ±1.2KHz、±2.4KHz、±3.6KHz、±4.8KHz、±6.0KHz. The ±1.2KHz bandwidth is recommended configuration during searching valid station.

FLT_SEL<2:0> register will affect the value of MW SNR. The narrow the bandwidth can get the high SNR value.

Registers	Address	Default Value	Access	Recommended Value
FLT_SEL<2:0>	0x62<2:0>	1	Read/Write	1

40 Base band AGC (BBAGC) in MW mode

MW of BBAGC controlled by five registers, as shown in Figure 18, MW_VOLUME<3:0> is used to set the volume gain, MW_BBAGC_HI_TH<5:0> determine BBAGC starting point, MW_BBAGC_RATIO<2:0> determine the slope of the volume with the power of changing, MW_BBAGC_LOW_TH<5:0> determine BBAGC termination point, when the transmission power is below it, the volume change with the transmit power is fixed 1:1 ratio, MW_BBAGC_BW<2:0> is used to control BBAGC change speed.

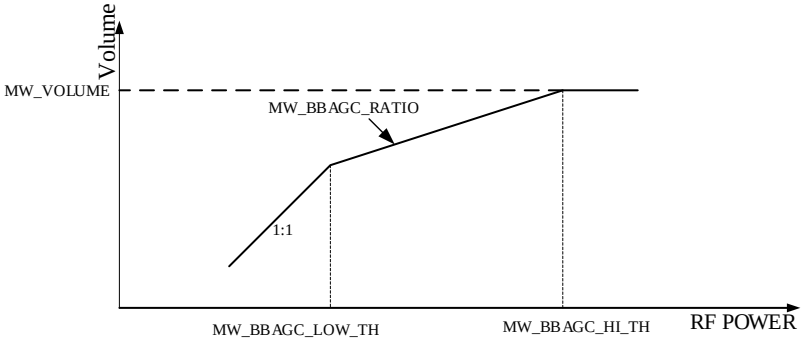


Figure 18: Illustration MW BBAGC

Registers	Address	Default Value	Access	Recommended Value
MW_VOLUME<3:0>	0x69<3:0>	10	Read/Write	10
MW_BBAGC_RATIO<2:0>	0x65<6:4>	5	Read/Write	5
AM_BBAGC_BW<2:0>	0x65<2:0>	0	Read/Write	7
MW_BBAGC_HI_TH<5:0>	0x67<5:0>	0x1B	Read/Write	0x1B
MW_BBAGC_LOW_TH<5:0>	0x68<5:0>	0x16	Read/Write	0x16

41 MW selective

MW selectively enhance will be enabled when register AM_SEL_ENHANCE=1.

Registers	Address	Default Value	Access	Recommended Value
AM_SEL_ENHANCE	0x2F<0>	0	Read/Write	1

SW Part

42 Setting SW band

Register AM_FM is used to set the working band, when CHANGE_BAND=1 means switching band is successful. After that the register CHANGE_BAND will be cleaned into 0 by the device.

The steps of switching band are as followed:

1) Shut down the ADC of CH pin.
2) Set the band range of SW, which means register LOW_CHAN<14:0>, register CHAN_NUM<11:0> and register AM_HIGH_CHAN<14:0> must be configured.
3) Setting FM frequency step SW_SPACE<1:0>.
4) Setting CH_GUARD<7:0>.
5) Setting register CH_ADC_WIN<12:0>
6) Set register AM_FM=1 and register CHANGE_BAND=1, KT0937 can be working in SW channel mode.
7) Turn on the ADC of CH pin.
8) KT0937 will adjust to the channel that corresponding to CH potential device, after switching successful.

Registers	Address	Default Value	Access	Recommended Value
CH_ADC_DIS	0x71<7>	0	Read/Write	-
CH_ADC_START	0x71<2>	0	Read/Write	-
LOW_CHAN<14:8>	0x98<6:0>	0x01	Read/Write	-
LOW_CHAN<7:0>	0x99<7:0>	0xF8	Read/Write	-
CHAN_NUM<11:8>	0x9A<3:0>	0	Read/Write	-
CHAN_NUM<7:0>	0x9B<7:0>	0x86	Read/Write	-
AM_HIGH_CHAN<14:8>	0x8C<6:0>	1	Read/Write	-
AM_HIGH_CHAN<7:0>	0x8D<7:0>	0xF8	Read/Write	-
SW_SPACE<1:0>	0x19<1:0>	1	Read/Write	1
CH_GUARD<7:0>	0xA0<7:0>	0x17	Read/Write	-
CH_ADC_WIN<12:8>	0x74<4:0>	1	Read/Write	-
CH_ADC_WIN<7:0>	0x75<7:0>	0x14	Read/Write	-
AM_FM	0x88<6>	1	Read/Write	1
CHANGE_BAND	0x88<7>	0	Read/Write	1

43 Setting SW band range

In SW mode, you can set the start channel by register LOW_CHAN<14:0> and the register AM_HIGH_CHAN<14:0> can be set the end channel. The channel number can be set by register CHAN_NUM<11:0> and the frequency step can be set by register SW_SPACE<1:0>.

The calculation methods are as followed:

LOW_CHAN<14:0> = Channel start frequency (KHz) / 1 (KHz) **Equal 8**

AM_HIGH_CHAN<14:0> = Channel end frequency (KHz) / 1 (KHz) **Equal 9**

CHAN_NUM<11:0> = (Channel end frequency - Channel start frequency) / Frequency step (KHz) **Equal 10**

Example：set the channel band as 12000-13000MHz, and the frequency step 5KHz.

1) 12000KHz / 1KHz = 12000, which is 0x2EE0 in Hex, write 0xE0 into LOW_CHAN<7:0> while write 0x2E into LOW_CHAN<14:8>.
2) 13000KHz / 1KHz = 13000, which is 0x32C8 in Hex, write 0xC8 into AM_HIGH_CHAN<7:0> and write 0x032 into AM_HIGH_CHAN<14:8>.
3) (13000KHz - 12000KHz) / 5KHz = 200, which is 0x00C8 in Hex, write 0xC8 into CHAN_NUM<7:0> then write 0x00 into CHAN_NUM<11:8>.

Registers	Address	Default Value	Access	Recommended Value
LOW_CHAN<14:8>	0x98<6:0>	0x01	Read/Write	-
LOW_CHAN<7:0>	0x99<7:0>	0xF8	Read/Write	-
CHAN_NUM<11:8>	0x9A<3:0>	0	Read/Write	-
CHAN_NUM<7:0>	0x9B<7:0>	0x86	Read/Write	-
AM_HIGH_CHAN<14:8>	0x8C<3:0>	1	Read/Write	-
AM_HIGH_CHAN<7:0>	0x8D<7:0>	0xF8	Read/Write	-
SW_SPACE<1:0>	0x19<1:0>	1	Read/Write	1

44 SW frequency difference

Due to the accuracy of the crystal, there is a difference of the receiving frequency of KT0937-D8. If the accuracy of the crystal is 50ppm, the difference is about 50 Hz when receive the 1MHz signal. Frequency difference correction function can be turned off when the register SW_AFCD set to 1. The register SW_TH_AFC<2:0> decides the maximum range of correctable. SW frequency difference is calculated as follows:

SW frequency difference = | AFC_AAF<7:0> - AM_CARRIER_OFST<7:0> | * 128Hz

KT0937-D8 can detect the difference between the set frequency and the actual radio frequency, KT0937-D8 will correct when difference is less than SW_TH_AFC<2:0> threshold.

AFC_AAF<7:0> register indicates the current AFC correction amount, the unit is 128Hz.

The register AM_CARRIER_OFST<7:0> indicates that the difference between the corrected frequency and the actual radio frequency, the unit is 128Hz.

The Examples of SW frequency difference: the actual radio frequency is 10000KHz when frequency receiver is 10000.640KHz. Frequency correction process is shown in Figure 15. The register AFC_AAF<7:0> is 2 (256 Hz), the register AM_CARRIER_OFST<7:0> is -3 (-384 Hz). AM frequency difference = 2 * 128 - (-3 * 128) = 640Hz.

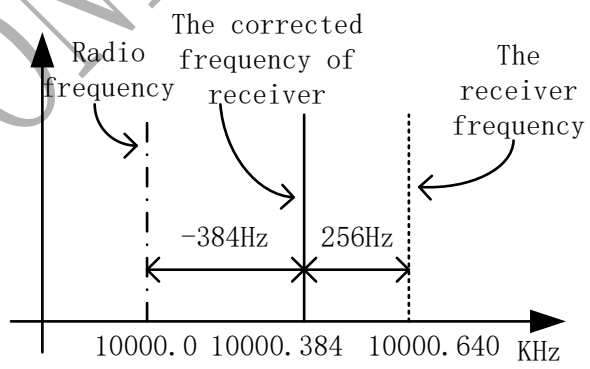


Figure 19: SW frequency difference

Registers	Address	Default Value	Access	Recommended Value
SW_AFCD	0x38<7>	0	Read/Write	0
SW_TH_AFC<2:0>	0x55<5:3>	0	Read/Write	3
AFC_AAF<7:0>	0x79<7:0>	0	Read Only	-
AM_CARRIER_OFST<7:0>	0xE8<7:0>	0	Read Only	-

45 Reading the current frequency in SW mode

You can get the current frequency by reading the value of the register RDCHAN<11:0>. In SW mode, the unit is 1KHz. The calculate method is as follows:

The current frequency (KHz) = RDCHAN<11:0>.

Registers	Address	Default Value	Access
RDCHAN<11:8>	0xE4<3:0>	0	Read Only
RDCHAN<7:0>	0xE5<7:0>	0	Read Only

46 RF signal strength indicator in SW mode

AM_RSSI<6:0> register is used to indicate the value of the RF signal strength of the current station in SW mode. The range of register value is 0-0x78. The register value 0 indicates -110dBm. 0x78 means 10dBm signal.

Calculated as follows:
SW RF signal strength (dBm) = AM_RSSI<6:0> - 110
SW RF signal strength (dBuV) = AM_RSSI<6:0> - 3
SW RF signal strength (dBuVEMF) = AM_RSSI<6:0> + 3

Registers	Address	Default Value	Access
AM_RSSI<6:0>	0xEA<6:0>	0	Read Only

47 SNR meter in SW mode

In SW mode, by reading AM_SNR_MODE1<6:0>register value can be obtained SNR of the current station. SNR is the worst when the value is 0. SNR is the best when the value is 0x7F.

FLT_SEL<2:0> register configuration will affect the SNR. The SNR will be higher when the bandwidth is narrower.

Registers	Address	Default Value	Access
AM_SNR_MODE1<6:0>	0xEC<6:0>	0	Read Only

48 SW valid station

In SW mode, valid tune module is used to judge whether the current receive channel is valid tune. There are three judgment conditions:

- ✧ The condition RSSI should meet.
  In SW mode, the RSSI value can be read from register AM_RSSI<6:0>, the RSSI threshold is depend on register SW_TUN_RSSI_HITH<6:0> and SW_TUN_RSSI_LOWTH<6:0>. When the RSSI value is bigger than the high threshold SW_TUN_RSSI_HITH<6:0>, it meets the condition. When the RSSI value is smaller than the low threshold SW_TUN_RSSI_LOWTH<6:0>, it does not meet the condition. When the RSSI value is between the high threshold SW_TUN_RSSI_HITH<6:0> and the low threshold SW_TUN_RSSI_LOWTH<6:0>, whether it meets the condition according to the last judgment, and it is a hysteretic interval.

- ✧ The condition SNR should meet.
  In SW mode, the SNR value can be read from register AM_SNR_MODE1<6:0>, the SNR threshold is depend on register SW_TUN_SNR_HITH<6:0> and SW_TUN_SNR_LOWTH<6:0>. When the SNR value is bigger than the high threshold SW_TUN_SNR_HITH<6:0>, it meets the condition. When the SNR value is smaller than the low threshold SW_TUN_SNR_LOWTH<6:0>, it does not meet the

condition. When the SNR value is between the high threshold SW_TUN_SNR_HITH<6:0> and the low threshold SW_TUN_SNR_LOWTH<6:0>, whether it meets the condition according to the last judgment, and it is a hysteretic interval.

✧ The condition uncorrected frequency difference should meet.
In SW mode, the uncorrected frequency difference can be read from register AM_CARRIER_OFST<7:0>, the unit is 128Hz. When uncorrected frequency difference is bigger than 3KHz, it does not meet the condition. When uncorrected frequency difference is smaller than 2KHz, it meets the condition. When the uncorrected frequency difference is between 2KHz and 3Khz, whether it meets the condition according to the last judgment, that is it is a hysteretic interval.

If the three conditions are all met, it is a valid tune VALID_TUNE=1. Otherwise it is an invalid tune VALID_TUNE=0. The judgment flow is as flowing:

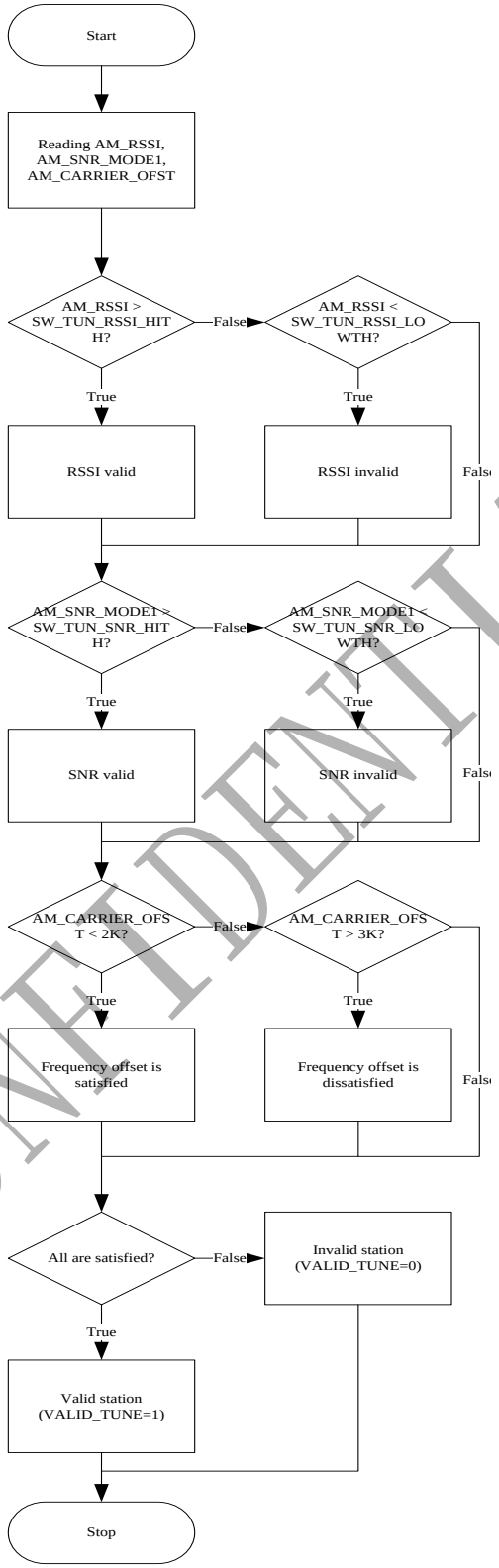


Figure 20: Flow chart of SW valid tune judgment

Registers	Address	Default Value	Access	Recommended Value
SW_TUN_RSSI_HITH<6:0>	0xF2<6:0>	0x24	Read/Write	0x24
SW_TUN_RSSI_LOWTH<6:0>	0xF3<6:0>	0x1F	Read/Write	0x1F
SW_TUN_SNR_HITH<6:0>	0xF0<6:0>	0x3A	Read/Write	0x3A
SW_TUN_SNR_LOWTH<6:0>	0xF1<6:0>	0x35	Read/Write	0x35
AM_RSSI<6:0>	0xEA<6:0>	0	Read only	-
AM_SNR_MODE1<6:0>	0xEC<6:0>	0	Read only	-
AM_CARRIER_OFST<7:0>	0xE8<7:0>	0	Read only	-
VALID_TUNE	0xDE<2>	0	Read only	-

49 Softmute setting of SW mode

When the quality of the input RF signal deteriorates, the output audio quality cannot be guaranteed. Sometimes, there could be harsh noise or broken sound. In such cases, users would be less annoyed if the audio volume could be reduced. KT0937-D8 offers the function of SOFTMUTE, which automatically decreases the audio volume when the quality of the input signal deteriorates, to improve the experience of the users, as in Figure 17.

The function of SOFTMUTE is enabled by setting the register SW_DSMUTE to 0. The attenuation of the volume is controlled by the RSSI, the SNR, and the register SW_SMUTE_MIN_GAIN<2:0>. KT0937-D8 calculates two values of volume attenuation, which are determined by RSSI and SNR separately. Then the two values are added in dB. Finally, the sum is saturated by the value set by the register SW_SMUTE_MIN_GAIN<2:0>, which will determine the actual volume attenuation, as shown in the point 11 of Figure 17.

The value of volume attenuation determined by SNR is calculated as follows. When the SNR of the input RF signal is less than the value set by the register SW_SMUTE_START_SNR<6:0>, the volume attenuation is enabled, as shown in the point 1 of Figure 17. While, the value set by the register SW_SMUTE_SLOPE_SNR<2:0> represents the slope of the attenuation. In this case, the attenuation should not be greater than 12dB, as in the point 2 of Figure 17.

The value of volume attenuation determined by RSSI is calculated as follows. When the RSSI of the input RF signal is less than the value set by the register SW_SMUTE_START_RSSI<6:0>, the volume attenuation is enabled, as shown in the point 5 of Figure 17. While, the value set by the register SW_SMUTE_SLOPE_RSSI<2:0> represents the slope of the attenuation. In this case, the attenuation should not be greater than 21dB, as in the point 6 of Figure 17.

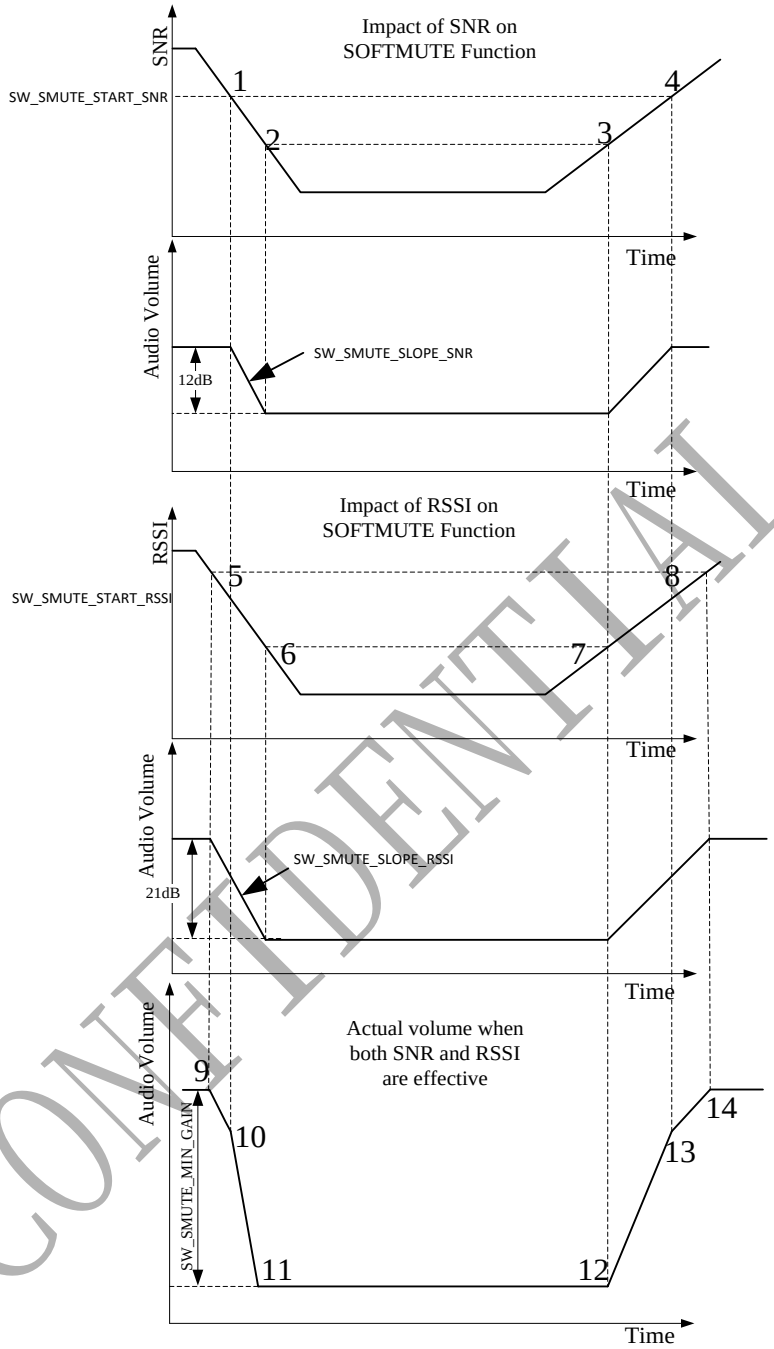


Figure 21: Illustration of SOFTMUTE in SW mode

Registers	Address	Default Value	Access	Recommended Value
SW_DSMUTE	0xF4<7>	0	Read/Write	0
SW_SMUTE_START_RSSI<6:0>	0xF5<6:0>	0x17	Read/Write	0x17
SW_SMUTE_SLOPE_RSSI<2:0>	0xF6<2:0>	4	Read/Write	4
SW_SMUTE_START_SNR<6:0>	0xF4<6:0>	0x30	Read/Write	0x30
SW_SMUTE_SLOPE_SNR<2:0>	0xF6<5:3>	0	Read/Write	0
SW_SMUTE_MIN_GAIN<2:0>	0xF7<5:3>	1	Read/Write	1

50 SW IF filter bandwidth configuration

The FLT_SEL<2:0> register is used to adjust the bandwidth of intermediate frequency filter in SW receiver. The narrow bandwidth of filter helps to suppress adjacent channel interference and reduce noise. It can improve audio SNR when RF signal is weak or there are some strong interference signals. If the narrow bandwidth of filter is used, the high frequency component of audio signal will be attenuate and there is a poor frequency response.

User can configure the FLT_SEL<2:0> register to obtain the different bandwidth of intermediate frequency filter, such as ±1.2KHz、±2.4KHz、±3.6KHz、±4.8KHz、±6.0KHz. The ±1.2KHz bandwidth is recommended configuration during searching valid station.

FLT_SEL<2:0> register will affect the value of SW SNR. The narrow the bandwidth can get the high SNR value.

Registers	Address	Default Value	Access	Recommended Value
FLT_SEL<2:0>	0x62<2:0>	1	Read/Write	1

51 Base band AGC (BBAGC) in SW mode

SW of BBAGC controlled by five registers, as shown in Figure 18, SW_VOLUME<3:0> is used to set the volume gain, SW_BBAGC_HI_TH<5:0> determine BBAGC starting point, SW_BBAGC_RATIO<2:0> determine the slope of the volume with the power of changing, SW_BBAGC_LOW_TH<5:0> determine BBAGC termination point, when the transmission power is below it, the volume change with the transmit power is fixed 1:1 ratio, AM_BBAGC_BW<2:0> is used to control BBAGC change speed.

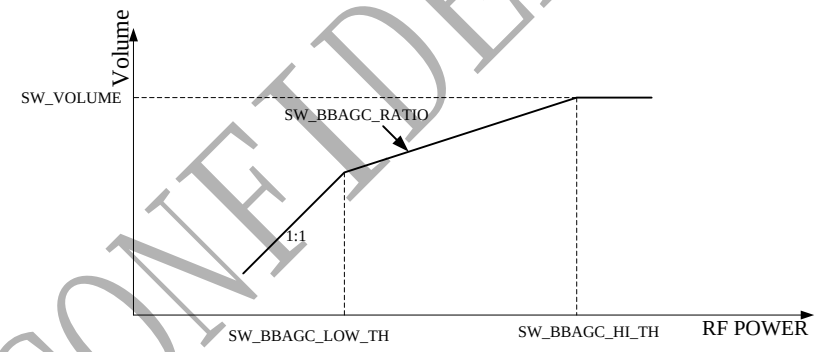


Figure 22: Illustration of BBAGC in SW mode

Registers	Address	Default Value	Access	Recommended Value
SW_VOLUME<3:0>	0x39<3:0>	10	Read/Write	10
SW_BBAGC_RATIO<2:0>	0x38<6:4>	4	Read/Write	4
AM_BBAGC_BW<2:0>	0x65<2:0>	0	Read/Write	7
SW_BBAGC_HI_TH<5:0>	0x3A<5:0>	0x1B	Read/Write	0x1B
SW_BBAGC_LOW_TH<5:0>	0x52<5:0>	0x16	Read/Write	0x16

52 SW selective

SW selectively enhance will be enabled when register AM_SEL_ENHANCE=1.

Registers	Address	Default Value	Access	Recommended Value
AM_SEL_ENHANCE	0x2F<0>	0	Read/Write	1

Appendix：

SMUTE_GAIN<7:0>	Attenuation
0x80	0.00
0x7F	-0.07
0x7E	-0.14
0x7D	-0.21
0x7C	-0.28
0x7B	-0.35
0x7A	-0.42
0x79	-0.49
0x78	-0.56
0x77	-0.63
0x76	-0.71
0x75	-0.78
0x74	-0.86
0x73	-0.93
0x72	-1.01
0x71	-1.08
0x70	-1.16
0x6F	-1.24
0x6E	-1.32
0x6D	-1.40
0x6C	-1.48
0x6B	-1.56
0x6A	-1.64
0x69	-1.72
0x68	-1.80
0x67	-1.89
0x66	-1.97
0x65	-2.06
0x64	-2.14
0x63	-2.23
0x62	-2.32
0x61	-2.41
0x60	-2.50
0x5F	-2.59
0x5E	-2.68
0x5D	-2.77
0x5C	-2.87
0x5B	-2.96
0x5A	-3.06
0x59	-3.16
0x58	-3.25
0x57	-3.35

0x56	-3.45
0x55	-3.56
0x54	-3.66
0x53	-3.76
0x52	-3.87
0x51	-3.97
0x50	-4.08
0x4F	-4.19
0x4E	-4.30
0x4D	-4.41
0x4C	-4.53
0x4B	-4.64
0x4A	-4.76
0x49	-4.88
0x48	-5.00
0x47	-5.12
0x46	-5.24
0x45	-5.37
0x44	-5.49
0x43	-5.62
0x42	-5.75
0x41	-5.89
0x40	-6.02
0x3F	-6.16
0x3E	-6.30
0x3D	-6.44
0x3C	-6.58
0x3B	-6.73
0x3A	-6.88
0x39	-7.03
0x38	-7.18
0x37	-7.34
0x36	-7.50
0x35	-7.66
0x34	-7.82
0x33	-7.99
0x32	-8.16
0x31	-8.34
0x30	-8.52
0x2F	-8.70
0x2E	-8.89
0x2D	-9.08
0x2C	-9.28
0x2B	-9.47

0x2A	-9.68
0x29	-9.89
0x28	-10.10
0x27	-10.32
0x26	-10.55
0x25	-10.78
0x24	-11.02
0x23	-11.26
0x22	-11.51
0x21	-11.77
0x20	-12.04
0x1F	-12.32
0x1E	-12.60
0x1D	-12.90
0x1C	-13.20
0x1B	-13.52
0x1A	-13.84
0x19	-14.19
0x18	-14.54
0x17	-14.91
0x16	-15.30
0x15	-15.70
0x14	-16.12
0x13	-16.57
0x12	-17.04
0x11	-17.54
0x10	-18.06
0xF	-18.62
0xE	-19.22
0xD	-19.87
0xC	-20.56
0xB	-21.32
0xA	-22.14
0x9	-23.06
0x8	-24.08
0x7	-25.24
0x6	-26.58
0x5	-28.16
0x4	-30.10
0x3	-32.60
0x2	-36.12
0x1	-42.14
0x0	mute

Revision History:

V1.0 First release.
V1.1 Modified section 13, 16, 29 and 42.
Added section 14 and 15.
V2.0 Modified register value.
Modified Figure 1and Figure 6.
V2.1 Modified section 21,25,26,27,29,30,31,35,40,43,44,48,49,50 and 51.