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QST Issue: Jun 1982
Title: Digital CMOS Iambic Keyer, A
Author: Ted Theroux, N9BQ

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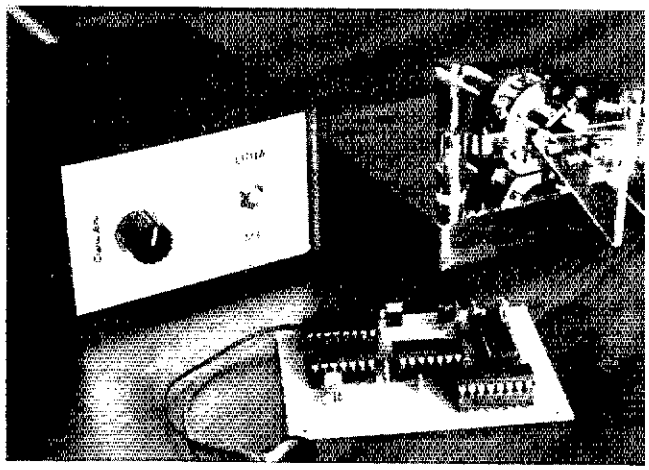
A Digital CMOS Iambic Keyer



After reading the theory on this keyer circuit you may exclaim, "Why didn't *I* think of that!" Simple CMOS circuitry provides expensive performance at low cost.

By Ted Theroux,* N9BQ

This CMOS keyer contains only five ICs and still has features such as iambic and electronic bug operation, dot and dash memories, perfect weighting, 9-volt battery operation, solid-state positive and negative output keying, no ON/OFF switch and low cost. It can be built in one evening.

Theory of Operation

The heart of this keyer is a two-bit binary counter. This counter has four possible output values or states: 0, 1, 2 and 3. The state of the counter is decoded to determine if the transmitter is to be on or off. During state 0, the transmitter will be off. When sending a dot, the counter will go to state 1 and then return to state 0; during a dash it will go through states 1, 2 and 3 before returning to state 0 (see Fig. 1). These state loops establish a perfect dot/dash/space ratio of 1:3:1. Each state is entered for one time unit, and the length of the time unit is determined by the setting of the SPEED control.

To make the following explanation easier to follow, the keyer has been broken down into 10 sections (see Fig. 2). The input filter consists of bypass capacitors C1 and C2, and pull-up resistors R1 and R2. An iambic paddle is connected to it at points labeled INDOT and INDASH. Paddle closure will pull these inputs to ground.

Dot and dash memories are made up of U1, a quad dual-input NAND gate. These gates make two flip-flops, whose outputs are DOTM for the dot memory and DASHM for the dash memory. Grounding inputs INDOT or INDASH will set the dot and dash flip-flops, respectively. Each memory will be cleared by the memory-clear gate after its respective cycle is completed.

U2B is the sequence control flip-flop. This flip-flop is clocked on the transition from state 0 to state 1. The J and K inputs are connected to DOTM and DASHM, the dot/dash memory outputs. The output SEQ will be clocked high if DOTM is active, low if DASHM is active, and alternate high and low if both are active. The sequence control flip-flop will determine if a dot or dash cycle will be entered. If SEQ is high, a dot cycle will be made — if low, a dash cycle. Outputs SEQ and $\overline{\text{SEQ}}$ enable memory-clear gates U3A and U3D, respectively.

The memory-clear gates, U3A and U3D, will gate the memory-clear pulses (CLP) from U2A pin 1 to clear the dot and dash memories. If SEQ is high, the dot memory will be cleared; if $\overline{\text{SEQ}}$ is high, the dash memory will be cleared.

U4A is the clock-control gate. The input pins are connected to the output of the dot and dash memories. If either input DOTM or DASHM is high, the output will go low, removing the STOP signal from the clock and the counter.

The clock circuit consists of U4B and U4C, capacitor C3, resistor R3 and potentiometer R7. The clock output is forced low when the STOP signal is high.

Memory-clear pulses are generated by U2A and U3C. Pulses will only be generated when the keyer is in state 0 and the clock is on its rising edge. During state 0, S$\emptyset\emptyset$ will be low, causing U3C pin 10 to go high. With U2A pin 6 high, the rising edge of the clock at U2A pin 3 will cause pin 1 of U2A to go high. Since pin 1 is connected to the clear input of U2A, the flip-flop will clear itself once it is set. Therefore, CLP will be a very short positive pulse.

The state counter consists of U5 and U4D. Pin 1 of U5A carries the most significant bit (MSB) of the two-bit binary counter, and pin 15 of U5B carries the least significant bit (LSB) of the counter. These signals are labeled M and L, respectively. The state of the counter will change on the rising edge of the clock. The counter state is determined by the input to U4D pin 13. If this input is high, the count will be 1, 0; if it is low, the count will be 1, 2, 3, 0.

An output decoder, U3B, decodes the value of the counter. Its output is low during state 0 and high during state 1, 2 and 3. The output driver is used to convert the CMOS logic level of the state decoder to an output capable of switching a positive or negative voltage to ground.

An Example

Operation of the keyer will be explained by using the letter "A" as an example. Use the schematic diagram in Fig. 3 and the timing diagram in Fig. 4 as references. A "1" will indicate a high logic level, and a "0" will indicate a low level.

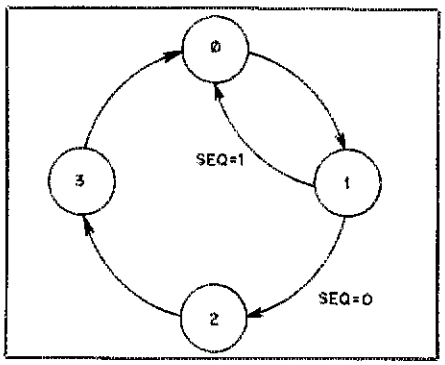


Fig. 1 — Logic state diagram for the keyer. Sequence 1 represents dot generation, and sequence 0 represents dash generation.

*26148 W. Mary Anne Rd., Antioch, IL 60002

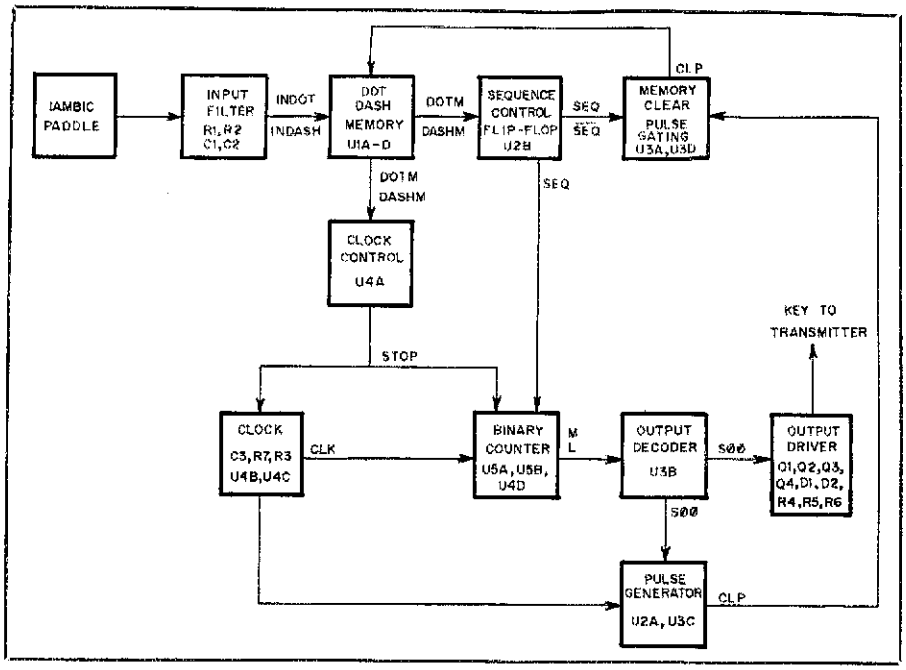


Fig. 2 — A binary counter forms the "heart" of the keyer design. See text for details.

When the keyer is in the idle state, it will be in state 0, with M = 0 and L = 0. The STOP signal is high since both the outputs of the dot and dash memories are low. The STOP signal forces the clock to a low level and enables the clear inputs to the counter — U5 pins 4 and 12.

For the letter "A," the dot paddle is activated, followed by the dash paddle, and then both are released. Let's begin by examining the operation of the keyer from the moment the dot paddle is initially depressed. The paddle pulls the INDOT signal low, which causes the dot memory to be set. DOTM will go high. With DOTM high, STOP will go low and the CLK will go high. The first rising edge of the clock will increment the counter to a count of one; therefore, L = 1 and $\overline{L}$ = 0. With U3B pin 6 low, SØØ will go high, turning on the output driver and keying the transmitter. The U2B clock input is clocked on the low to high transition of the SØØ signal. With DOTM = 1 and DASHM = 0, SEQ will go high, thus enabling the next clear pulse to be gated to the dot memory through U3D.

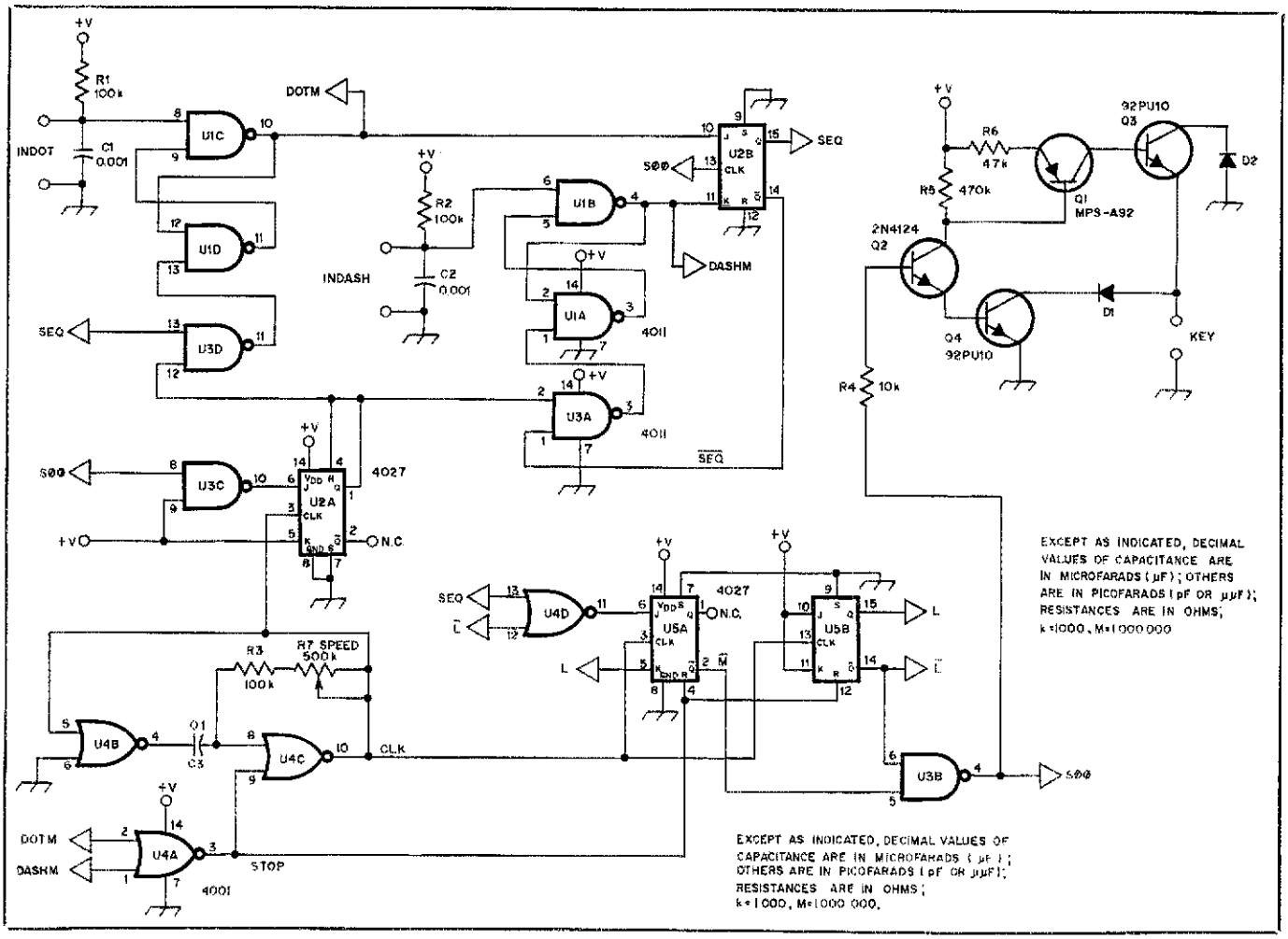


Fig. 3 — Digital CMOS keyer schematic diagram. All resistors are 1/4-watt, carbon-composition types. Capacitors are disc-ceramic 50-volt units, unless otherwise specified.

C1, C2 — 0.001 μF.
C3 — 0.1 μF.
D1, D2 — 1N4004 silicon diode.
Q1 — MPSA92.
Q2 — 2N4124.
Q3, Q4 — 92PU10 npn silicon medium-power. V_{ceo} = 300 V, IC = 30 mA and V_{cb} = 300 V.
U1, 3 — 4011 CMOS quad two-input NAND gate.
U2, 5 — 4027 CMOS dual J-K flip-flop.
U4 — 4001 CMOS quad two-input NOR gate.

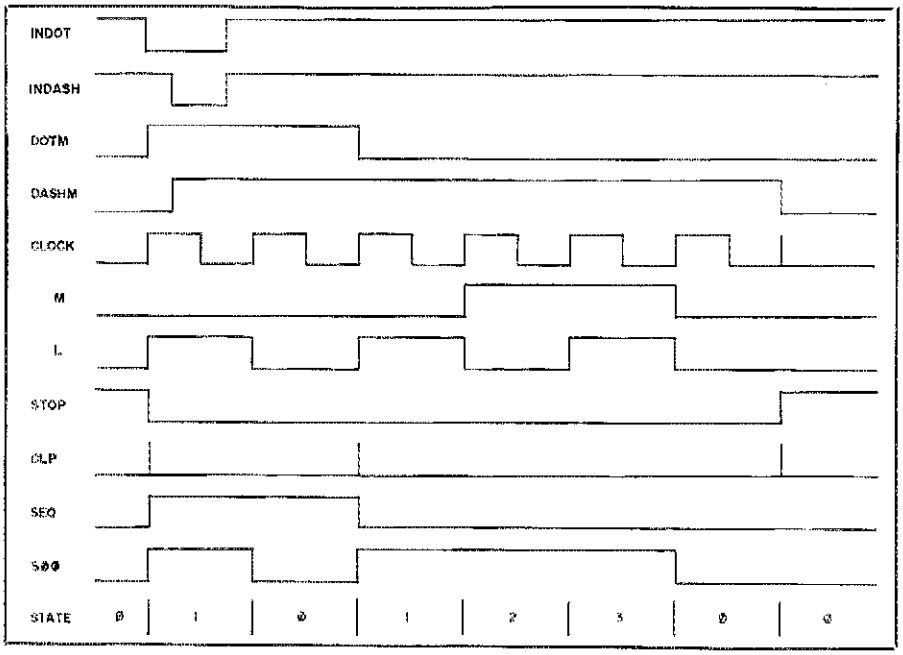


Fig. 4 — Timing diagram for the letter A. See text for details.

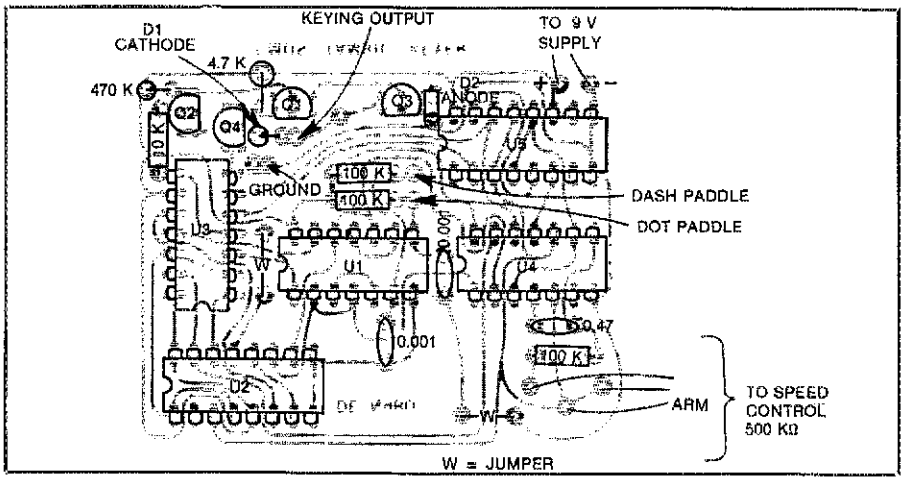


Fig. 5 — Parts-placement guide for the CMOS keyer. Parts are located on the nonfoil side of the board. The shaded area represents an X-ray view of the copper pattern.

With SEQ = 1, the J input to U5A pin 6 will be low. Therefore, on the second clock pulse, the counter will return to state 0 and the transmitter will be "unkeyed." Since the dash paddle was also depressed, DASHM = 1, which continues to disable the STOP signal and keeps the clock running. On the third clock pulse, a clear pulse generated by U2A (pin 1) is gated by U3D to clear the dot memory. The third clock pulse will also increment the counter to state 1, and again the transmitter will be keyed. On this second transition from state 0 to state 1, U2B will be clocked once again at pin 13. This time, since DOTM = 0 and DASHM = 1, the flip-flop will be reset and SEQ = 0. Now that SEQ = 0, the state counter will be enabled to go to state 2 on the fourth clock pulse, state 3 on the fifth clock pulse, and back to state 0 on the sixth clock pulse. Since the seventh clock pulse occurs during state 0, another clear pulse will be generated and, since $\overline{SEQ}$ = 1, the dash memory will be cleared through U3A. Now that DOTM = 0 and DASHM = 0, the STOP signal is enabled, the clock will be disabled, and the clear inputs to the state counter will be enabled.

Construction

All parts are mounted on a single printed-circuit board.[1] Other construction techniques such as point to point or wire wrapping can also be used. The keyer can be installed inside a small chassis box, or you may want to install it inside your rig. Power is supplied by a 9-volt battery or any dc source from + 7 to + 15 volts. The current drain in the key-down position is 2.5 mA at 9 volts. The output of the keyer is capable of switching voltages of + 300 V to − 300 V to ground with a maximum current of 55 mA.

For electronic bug operation, connect the dash side of the iambic paddle to the output of the keyer instead of to the DASHIN input. Do not connect the dash side of the paddle to both the DASHIN input and the output of the keyer at the same time. A switch could be added so you can select between iambic or bug operation. No rf shielding was used on the prototype, and no RFI problems have been encountered in the shack or in the field.

[1]Etched and drilled printed-circuit boards and complete parts kits are available for $12 and $25.95, respectively, postage paid from the author. The ARRL and *QST* do not warrant this offer in any way.

Strays

PALDEN THONDUP NAMGYAL, AC3PT

Palden Thondup Namgyal, AC3PT, the deposed King of Sikkim, died in New York in February 1982, following a prolonged illness. He was 58. The last Chogyal (maharaja) of Sikkim, Namgyal ruled that mountain kingdom on the southern slopes of the eastern Himalayas from 1964 to 1975, when he was forced to relinquish power and his kingdom was annexed by India.

SILENT SIDE OF MAXIM

☐ There is an interesting article about H. P. Maxim in the February issue of *The American Rifleman*. Although Maxim's Amateur Radio pursuits are largely ignored, the article describes his work in developing the Maxim Silencer. There are lots of photos of Hiram and his son, H. H. Maxim, who played an important role in the early days of ARRL and Amateur Radio.

I would like to get in touch with . . .

☐ someone who can provide a schematic for a Code-A-Phone model 1400 phone recorder. Lee Allen, WB4DOR, P.O. Box 444, Madison, TN 37115.

battery types and mounting methods have been suggested.

One alternative worth mentioning is the battery pack used for the Azden PCS-3000. This 4.8-V nickel-cadmium battery will fit conveniently in the control head. It is available from Amateur-Wholesale Electronics.[1] — *Larry Wolfgang, WA3VIL, ARRL Hq.*

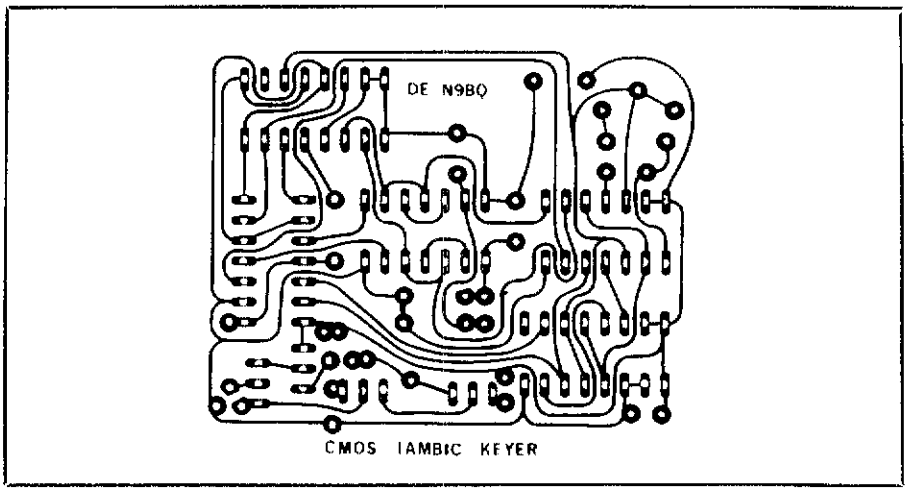
ICOM IC-730 CW FILTERS

☐ When I purchased an ICOM-IC-730, I also ordered the IC-EX203 cw audio filter. After installing the filter, according to the manufacturer's instructions, I was disappointed to find that the filter was actuated in both the CW and CW-N positions. I find that having a 150-Hz filter in the circuit at all times during cw operation is inconvenient. With minor circuit modifications, my audio filter is now active only when the MODE switch is in the CW-N position.

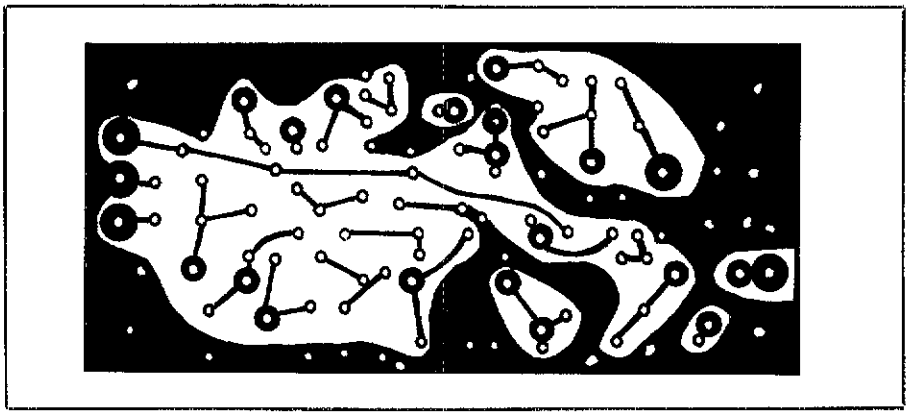
The first step is to fabricate a 5-inch length of wire with a flat pin on each end. The pins I used were removed from an IC socket found in my junkbox. Remove the green wire and the connector from P1, which plugs into J3 on the detector board. This wire goes to pin 1. Now install the filter board. One end of the wire fabricated earlier is plugged into the connector on the green wire removed from P1. The other end of this wire is soldered to the point on P6 that goes to J4 pin 2. I used a piece of plastic electrical tape to insulate these connections.

With the mode switch in the CW-N position, 8-V dc is supplied to the audio filter, turning it on. Now I have two bandwidth choices on cw, and operating is much easier. — *Robert Putnam, K7ACP, Roseburg, Oregon* QST☐

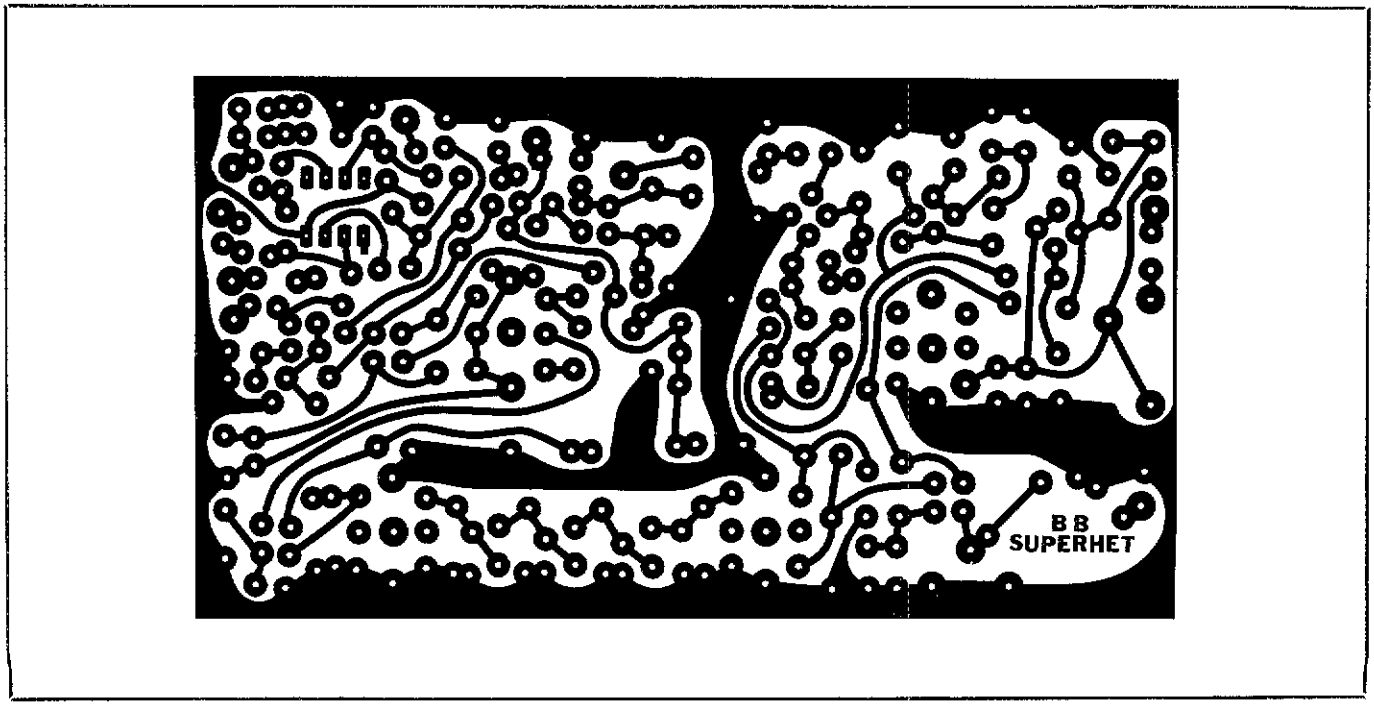
[1]Amateur-Wholesale Electronics, 8817 S.W. 129th Terr., Miami, FL 33176. The cost is $5.70, plus shipping. AWE will also supply a modification sheet, with details of how to install this battery, on request.



Circuit-board etching pattern for the CMOS keyer. Pattern is shown at actual size from the foil side of the board, with black representing copper. Copper is on one side only. The parts-placement diagram appears on page 28.



Etching pattern for the 6-meter receiving converter. Black areas represent unetched copper, viewed from the etched side of the board. Parts-placement diagram appears on page 43.



Scale etching pattern (foil side) of the Bare-Bones Receiver circuit board.