STEREO
how to design your own solid-state audio amplifier

Class AB power amplifiers

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THE QUANTITY OF POWER THAT CAN BE delivered by a Class-A amplifier is extremely limited. A transistor can dissipate a specific amount of power. Should the transistor conduct current over the entire cycle, as well as when it is idling, a considerable amount of power is wasted just keeping the device operating at its predetermined quiescent bias. This is the state of affairs in Class-A operation.

On the other hand, Class-B power amplifiers are biased so that no collector current flows when the transistor is idling. The transistor does not conduct until the applied signal is of such magnitude and polarity as to put the device into its active region. NPN transistors, for example, do not conduct until the signal applied to the base relative to the emitter, is positive and greater in magnitude than the 0.6 or 0.7 volt necessary to turn on the base-emitter junction.

Even though the amount of power dissipation in Class-B remains identical to its capabilities in Class-A, in Class-B the amplifier will dissipate this power only when conducting useful audio currents. The portion of power wasted in maintaining the Class-A bias is applied here to enable the Class-B amplifiers to deliver more useful signal output.

Only one half of a purely ac sinusoidal cycle will turn on a Class-B biased transistor. To reproduce the alternate half of the cycle, the circuit must use a second transistor to conduct during this latter portion of the cycle. Two transistors are required to reproduce a full cycle in Class-B-biased amplifier circuits.

Class-B statistics

A push-pull Class-B amplifier circuit is shown in Fig. 1 using two npn transistors. Should a sinewave be fed to the input, the various waveshapes shown can be found at the specific points in the circuit when they are measured with respect to ground. The dots next to the ends of the input transformer windings

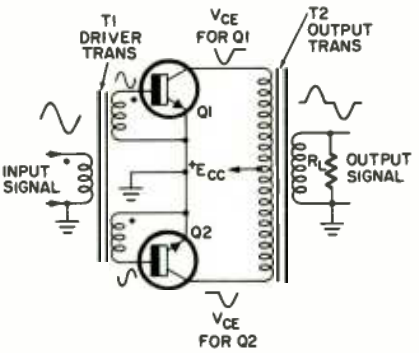

FIG. 1—TRANSFORMER-COUPLED Class-B push-pull circuit. Significant waveshapes are shown.

indicate that the corresponding leads or terminals are identical in polarity with respect to those at the unmarked ends. The base of Q1 is in phase with respect to its emitter as is the "hot" lead of the input signal with respect to ground. Establishing the proper status for push-pull operation, the polarity at Q2's base is 180° out of phase with that at Q1's base.

During the first half cycle, Q1's base is positive with respect to the emitter, so this transistor conducts. Q1 does not conduct during the second half cycle for during this interval, the base-emitter junction is reversed in polarity. The collector voltage is, as shown, for the voltage across the transistor and the upper half of the transformer winding is reduced as the transistor goes into conduction.

The second half of the cycle turns Q2 on; for only then does the signal bias that base positive with respect to the emitter. The waveform of the output voltage at the bottom of the output transformer with respect to the center tap, as well as across the transistor, is as shown. The voltage across the entire primary is relatively sinusoidal, as is the output signal across the load R_L. Ideally, the output signal is a magnified version, power-wise, of the input signal.

As discussed for the Class-A amplifier, the two transistors see the actual load R_L reflected as a resistor, R_L', into the *entire* primary winding of the output transformer T2. $R_L' = R_L(N_p/N_s)^2$ is an equation describing the relationship. In this formula, N_p is the number of turns in the *entire* primary winding and N_s is the number of turns in the secondary. Either one of the transistors sees a resistance, R_L'', across *one half* of the transformer winding. Since the number of turns each transistor sees is $N_p/2$, $R_L'' = R_L(\frac{N_p}{2}/N_s)^2 = (R_L/4)\ (N_p/N_s)^2$. Comparing the two equations, we arrive at the important conclusion that R_L'' is equal to $\frac{1}{4}R_L'$ or that the ac load seen by either *one* transistor appearing across *half* the primary winding of the transformer. is equal to one-fourth that seen by *both* transistors across the *entire* transformer.

Each transistor delivers power to the load. To determine the power delivered by two transistors. we need only determine the power one transistor delivers and multiply this number by two.

Using one transistor, draw the P_{CEM} maximum power dissipation hyperbola discussed last time. on the collector characteristic curves of the transistor. As was our previous practice, we omit the actual transistor curves to avoid cluttering the drawing. Assuming half the primary winding of T2 has zero resistance. the dc load line, defined by the equation $V_{CE} = E_{CC} - I_C R_P$, is a vertical line up from the E_{CC} voltage point on the V_{CE} axis. R_P in the equation is the resistance of $\frac{1}{2}$ of the primary winding of transformer T2.

The ac load resistance is $R_L'' = (R_L/4)\ (N_p/N_s)^2$. Assume that at its maximum, the load line is tangent to the P_{CEM} curve. (We will deviate from the concept of not working above the P_{CEM} curve later on. Here, we assume the load line cannot cross this hyperbola.)

If a sinusoidal signal is at the input, a half cycle of voltage and current appears at the output. For the maximum output, the collector to emitter voltage will swing from E_{CC} to zero and the

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collector current will swing from its I_{CM} maximum to zero. As the rms values of a half sinewave is the peak voltage or current divided by two, the signal power delivered to the ac load, R_L'', is

$$P_{R_L''} = \left(\frac{I_{CM}}{2}\right)\left(\frac{E_{CC}}{2}\right) = \frac{E_{CC}^2}{4R_L''} = \frac{I_{CM}^2 R_L''}{4} \quad (1)$$

This equation is valid irregardless of where the ac load line is with respect to the P_{CEM} hyperbola. The maximum power is dissipated by the transistor at the instant the swing is at the center of travel, or

$$P_C(\text{max}) = \left(\frac{I_{CM}}{2}\right)\left(\frac{E_{CC}}{2}\right) \quad (2)$$

This equation is also independent of the P_{CEM} curve. It should be emphasized that P_C(max) is not the average power the transistor will dissipate. It is the power the transistor will dissipate only at the instant the swing is at $I_{CM}/2$ and $E_{CC}/2$. This is the maximum power it will dissipate at any point in the swing. If the load line is tangent to the maximum allowable power dissipation hyperbola, P_C(max) is equal to P_{CEM}. The power dissipated when averaged over the entire cycle is less than P_C(max) for it is P_C(max) for but two instants in the half cycle as it swings on the load line.

Comparing equations 1 and 2, we note that the transistor can deliver as much power as the maximum instantaneous power it will dissipate in the half cycle. This is double the power the same transistor can deliver in the Class-A mode of operation.

The average or dc current in a half sinewave of collector current is I_{CM}/π. This was discussed in the article on rectification. The power supply must provide this dc current. It must provide $E_{CC}(I_{CM}/\pi)$ watts to the transistor. Comparing this with the power delivered to the load, the percent efficiency of the circuit is $100P_{R_L''}/P(\text{supply}) = 100\pi/4 = 78.5\%$—a decided improvement over the Class-A case.

The transistor dissipates power during ½ the cycle only for it does not conduct during the alternate half cycle. Over a complete cycle, one transistor of the push-pull pair will dissipate

$$P_{trans}(\text{for 1 cycle}) = 0.068E_{CC}^2/R_L'' \text{ watts} \quad (3)$$

if the signal swings the output from zero to its E_{CC} maximum limit. The average power the device will dissipate over the cycle, is higher if the swing is less than the maximum. Should the transistor deliver about 40% of the $P_{R_L''}$ in equation 1, it will dissipate more power than it will dissipate with any other size of signal swing. The power it will dissipate is

$$P_M(\text{av}) = V_{CC}^2/\pi^2 R_L'' \text{ watts} \quad (4)$$

if the power it delivers to the load is 40% of the maximum. Comparing this with equation 2, the transistor can deliver about 2½ times the power it may dissipate.

Averaged over a complete cycle, the transistor may dissipate P_{CEM} watts. It will cross the P_{CEM} hyperbola and yet be within the power dissipation rating of the transistor when the dissipation is averaged over the 360°. This differs from the Class-A case for here the idling and average power over the cycle were at P_{CEM} when the transistor was biased for minimum distortion. As the power during idling (and hence the average during the cycle) was not permitted to exceed P_{CEM}, the load line was not permitted above the maximum power dissipation hyperbola.

Class-B design procedure

Assume you want to design a 60-watt push-pull amplifier which will drive an 8-ohm speaker system. How would you proceed to specify the output transistors and transformer? Use the circuit in Fig. 1.

If the two transistors are to deliver 60 watts, each one must be capable of delivering half the power or 30 watts to the load. If the transformer is 25% efficient, the transistors must deliver 30 watts + 25% of 30 watts = 37.5 watts to the primary of half the output transformer. Add about 10% to compensate for losses due to saturation voltage and leakage current, so that the circuit should be designed to be capable of providing about 42 watts.

A good power transistor for this application is the 2N3055. The maximum collector current that can safely flow through this transistor is 10 amperes.

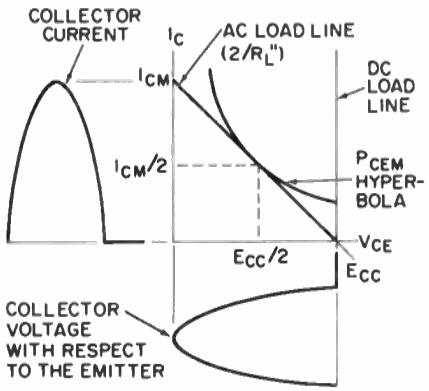

FIG. 2—PLOT OF LOAD lines for Class-B amplifier. A sinusoidal input and output signal is assumed.

FIG. 3—CURVES FOR CLASS-B design procedure.

Adding some leeway, use 6 amperes as the maximum collector current. As the rms current of the half sinewave (see Fig. 3) is 6/2 = 3 amperes, the load the transistor must see at the primary of the transformer is:

$R_L'' = P_{R_L''}/I_{rms}^2 = 42/9 = 4.66$ ohms

The supply voltage, from equation 1, is:

$E_{CC} = (4R_L'' P_{R_L''})^{\frac{1}{2}} = (4 \times 4.66 \times 42)^{\frac{1}{2}} = 28$ volts

Maximum power is dissipated by the transistor when the power delivered to the load is about 40% of 42 watts, or 16.8 watts. When delivering this power, the transistor dissipates $V_{CC}^2/\pi^2 R_L''$ watts = 783/(9.9)4.66 = 17 watts. The 2N3055 can easily cope with this power dissipation requirement.

(It is interesting to stop for a moment and note several things here. For the full swing, the transistor will dissipate $0.068V_{CC}^2/R_L'' = (0.068)(783)/4.66 = 11.4$ watts. This is less than the power dissipated when 40% of the maximum power is delivered to the load.

(The power a transistor will dissipate is equal to the power taken from the supply less the power delivered to the load. The power furnished by the supply can be calculated as follows. Based on equation 1, the square of the collector current swing is $I_C^2(40\%) = 4P_{R_L''}(40\%)/R_L''$ for the case where the output is 40% of maximum. Hence, $I_C^2(40\%) = 4(16.8 \text{ watts})/4.66 \text{ ohms} = 14.4 \text{ amperes}^2$. The current is then $I_C(40\%) = \sqrt{14.4} = 3.79$ Amperes. The power from the supply is $E_{CC}(I_C(40\%)/\pi) = 28(3.79/3.14) = 33.9$ watts. Subtract the 16.8 watts delivered to the output at 40% of the maximum output power from the 33.9 watts supplied by the power source, and the transistor must dissipate 17.1 watts. This is very close to the 17 watts solution determined from the $V_{CC}^2/\pi^2 R_L''$ equation above. This alternate method is presented to indicate a logical procedure used to determine the transistor power dissipation at any portion of the maximum power the device can deliver, rather than being required to memorize a nebulous formula.)

Since the impedance across one-half the primary of the output transformer is 4.66 ohms, the impedance from collector to collector, across the entire primary, is 4 x 4.66 ohms, or 18.64 ohms. The impedance ratio of the entire primary to the secondary is 18.64 ohms: 8 ohms —2.33:1. The turns ratio is the square root of the impedance ratio, or 1.51:1

Turning to Class-AB

A typical set of collector characteristic curves are in Fig. 4, for the 2N3055. Notice that they are not evenly spaced. Should the collector-current swing the full 10 amperes for the half cycle, the

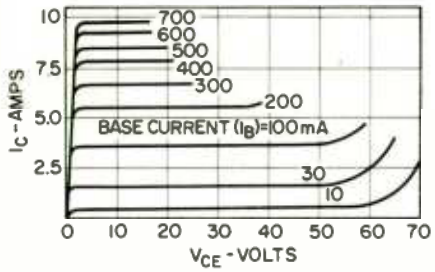

FIG. 4—TYPICAL OUTPUT characteristics of power transistors. Courtesy RCA

current gain differs at different points of the cycle. For example, at the point the in cycle where 2 amperes collector current is required, the base current at the input is about 40 ma. At the 4 ampere collector current point in the cycle, the base current is about 120 ma, while for 6 amperes, it is about 250 mA. In the portion of the output curve where there is a 2-ampere collector current rise from 2 to 4 amperes, the equivalent base current increase about 120 − 40 mA = 80 mA, while for the same 2-ampere collector current increment from 4 to 6 amperes, the equivalent base current increase 250 − 120 ma = 130 ma. Even though the increase in collector current remains at 2 amperes in both cases, the base current drive required was greater at higher collector currents. This information could, of course, have been derived from the beta curves which show that beta varies considerably with collector current. The a-c and d-c current gain is nonlinear producing distortion.

Another curve, shown in Fig. 5, is a

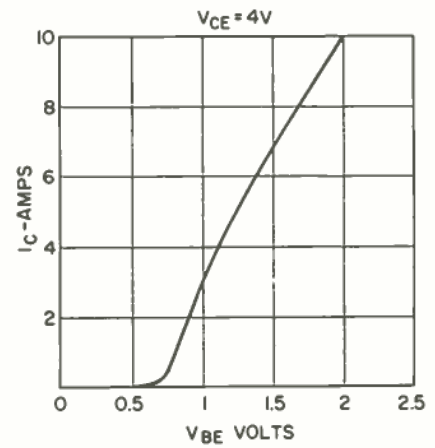

FIG. 5—TYPICAL TRANSFER characteristics of power transistors. Courtesy RCA

plot of the collector current against the base-emitter voltage. You may recognize this as a transconductance curve, where the definition of transconductance is not unlike that applied to the JFET. Notice that this curve, after the first 0.6 or 0.7 volts is a relatively straight line. The slope of this line is the a-c transconductance. It is equal to $\Delta I_C/\Delta V_{BE}$, where the Δ indicates a change or difference. The a-c transconductance is relatively constant with changes in collector current. Should the half cycle of 10 ampere collector current be at the output, the required input base-emitter voltage at the 2 ampere collector current point in the cycle is 0.9 volts, at the 4 ampere point it is 1.1 volt, and at 6 amperes it is 1.3 volts. While the collector current increase is in increments of 2 amperes, the base to emitter voltage increase in one case is 1.1 volts − 0.9 volts = 0.2 volts and in the second case it is 1.3 volts − 1.1 volts = 0.2 volts. Hence equal changes in base emitter voltages produce equal changes in collector current. This is a linear situation favorable to the cause of low distortion.

Good power amplifiers are driven from low impedance voltage sources where transconductance is the controlling factor, rather than high impedance current sources where the varying beta determines the relatively distorted output.

In Fig. 6-a, we apply half a sine wave of voltage to the input between the base and emitter. The collector current at the output appears next to the I_C axis. Note that there are portions in the cycle where there is little or no output current. This is known as the crossover region. For the two transistor push-pull circuit in Fig. 1, the output across the load, R_L, would appear as in Fig. 6-b rather than be perfectly sinusoidal. This signal has a considerable amount of odd harmonic distortion and intermodulation distortion. Even worse,

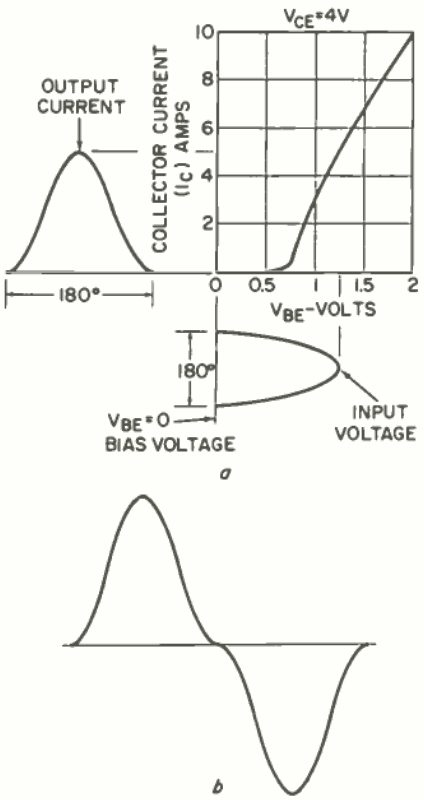

FIG. 6-a—COLLECTOR CURRENT due to half a sinewave input. b.—COLLECTOR CURRENT as it appears for a full cycle. Note crossover distortion. Courtesy RCA

in conjunction with transformer and speaker inductance, this abrupt crossover can cause sharp peaks in the circuit which can damage or destroy the transistor.

Crossover distortion can be minimized if the transistor is biased so that it is always conducting some minimal amount of collector current. A normal procedure to determine the minimum base-emitter voltage for this type of operation is to extend the straight line of the curve to the V_{BE} axis. The curve in Fig. 5 crosses this axis at 0.75 volts. The transistor should be biased at this voltage. It may be true that some power will be dissipated due to the idling collector current (about 40 mA at 0.75 volts), but the reduction in crossover distortion is well worth this minor expenditure of power. Some manufacturers cause the transistors to idle at much higher current to assure that the collector current will never be completely cut off. This type of biasing puts the transistor into what is referred to as Class-AB operation.

A drawing of the output current when the transistor is biased at 0.75 volts is shown in Fig. 7. There is no por-

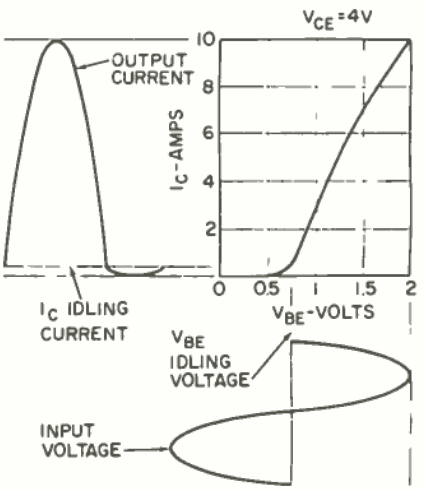

FIG. 7—CURVES WHEN TRANSISTOR is biased for Class AB operation. Courtesy RCA

tion of the half cycle during which there is an absence of collector current flow. The distortion is relatively low when compared to the Class-B mode of operation. The output over the full cycle is a relatively good sine wave.

Should the circuit in Fig. 1 be biased for Class-AB operation, it could take the form shown in Fig. 8. The bias voltage is developed across R_X, which is applied between the bases and emitters of the two transistors. R_B and R_X form a voltage divider with E_{BB} as the source of the base bias supply voltage. The quiescent base current can be determined using Thevenin's equivalent circuit procedures described in an earlier article. Do not forget to include the dc resistance of the driver transformer's

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