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Design a New Architecture of Audio Amplifier Class-D for Cellular Phones

Karim EL KHADIRI and Hassan QJIDAA

Sidi Mouhamed Ben Abbellah University
Faculty of Science Dhar El Mahrez
Laboratoire d'Electronique Signaux – Systèmes et Informatique (LESSI)
Fez, Morocco

Abstract

This paper presents a new architecture of class D audio amplifier with 0.4 W output power and 95% efficiency with an 8 ohm load. This class D uses a pulse width modulation scheme that eliminates the output filter. It operates with a 2.4 V to 5V supply voltage. The fully differential class-D audio amplifier is implemented with a TSMC 0.13-um 2P4M CMOS process, and the chip area is 325 x 300 um2. It has a THD as low as 0.04%, with a flatband response between 20 Hz and 20 kHz.

Keywords: Class-D Amplifier, H-Bridge, Triangle-wave generator, Pulse-width-modulation.

CORRESPONDING AUTHOR: *karim.elkhadiri@usmba.ac.ma, +212676548780*

I. INTRODUCTION

High power efficiency, small size and reduced heat dissipation are highly desirable in battery-powered mobile systems and switched-mode class-D amplifiers can readily satisfy these requirements. However, full adoption of class-D technology in mobile systems has been somewhat limited due to concerns such as signal distortion and noise, poor power supply noise rejection, electromagnetic interference (EMI) and the requirement for external LC filters.

The operation of class D amplifier was invented in 1959 by Baxandall, who suggested using LC oscillator. The motivating factor research in class D amplifier is efficiency. The efficiency of linear amplifier is 30–40% practically in spite of 78.5% theoretically. At the same time, it must increase the chip area or even add a plus radiating flange for the elimination of heat; thus too much area is taken and also the cost is unaffordable. When it comes to class D amplifier, since the output power metal–oxide semiconductor field effect transistors (MOSFETs) of class D amplifier operate in the triode and cut-off regions, the efficiency of class D is over 80% in practical application with 100% theoretic efficiency, which can greatly reduce the power dissipation, area of chip and printed circuit board (PCB) and cost. Therefore, class D amplifiers are becoming favourable in consumer electronic products such as DVD, LCD-TV, MP4 and cell phone[1], [2], [3], [4], [5][6],

The modulation techniques commonly applied for the realization of analog class D amplifiers include: (1) pulse-width-modulation (PWM) and (2) sigma–delta (∑D) modulation. Digital class D

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amplifiers are based on the similar modulation techniques. Among these tow modulation techniques; PWM is arguably most prevalent because it features the lowest quiescent current due to its lower switching frequency and hardware simplicity [6]. PWM inherently uses the fewest edges per unit time which introduces less noise and improves the switching efficiency, increasing resolution and maximum power output [7].The open-loop class D amplifier with conventional PWM modulation, which is shown in Figure1, compares the audio signal with internally generated carrier wave form at high frequency. Resultant wave forms area series of pulses, where the pulse width is proportional to amplitude of audio signal. The power stage driven by the PWM signal is used to provide sufficient current to drive a low-impedance load. However, a bulky LC low-pass filter is required to remove unwanted signal components of PWM, which increases the cost and volume, and suffers from nonlinearity [7], [8].

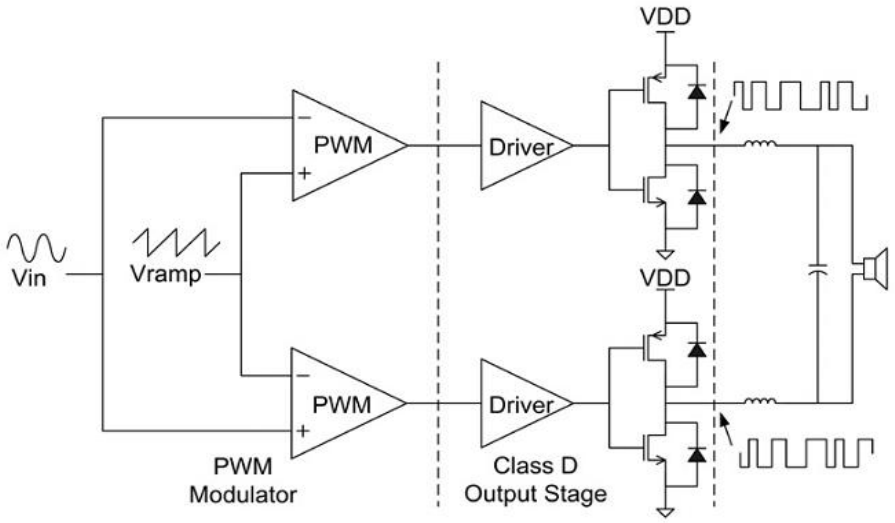

Fig. 1. Fig1. Open-loop PWM class D amplifier.

The proposed class D audio amplifier achieves a maximum power efficiency of 95% delivering up to 0.4W output power to load, and operates with a supply in the range 2.4–5.V. The total harmonic distortion plus noise (THD+N) is less than 0.1% between 20 and 20 kHz with output power 0.4W and the quiescent current without load is 0.6 mA. The design has been implemented with TSMC 0.13-um complementary metal–oxide–semiconductor (CMOS) process and occupies 325umX 300um.

In this paper, the circuit description of the proposed class-D amplifier is shown in Sect. II, and then the simulation results are shown in Sect. III. Finally, the conclusion is made in Sect. IV.

II. DESIGN THEORY OF HIGH-PERFORMANCE CLASS D AMPLIFIER

A. Design and analysis of the proposed architecture

The Design of a class D audio amplifier using PWM, which is shown in Figure 2, is mainly composed of four parts. The first part is the input circuit which consists of analog amplifier, generally receives the analog input signal from a source external to class-D amplifier. The second part is the

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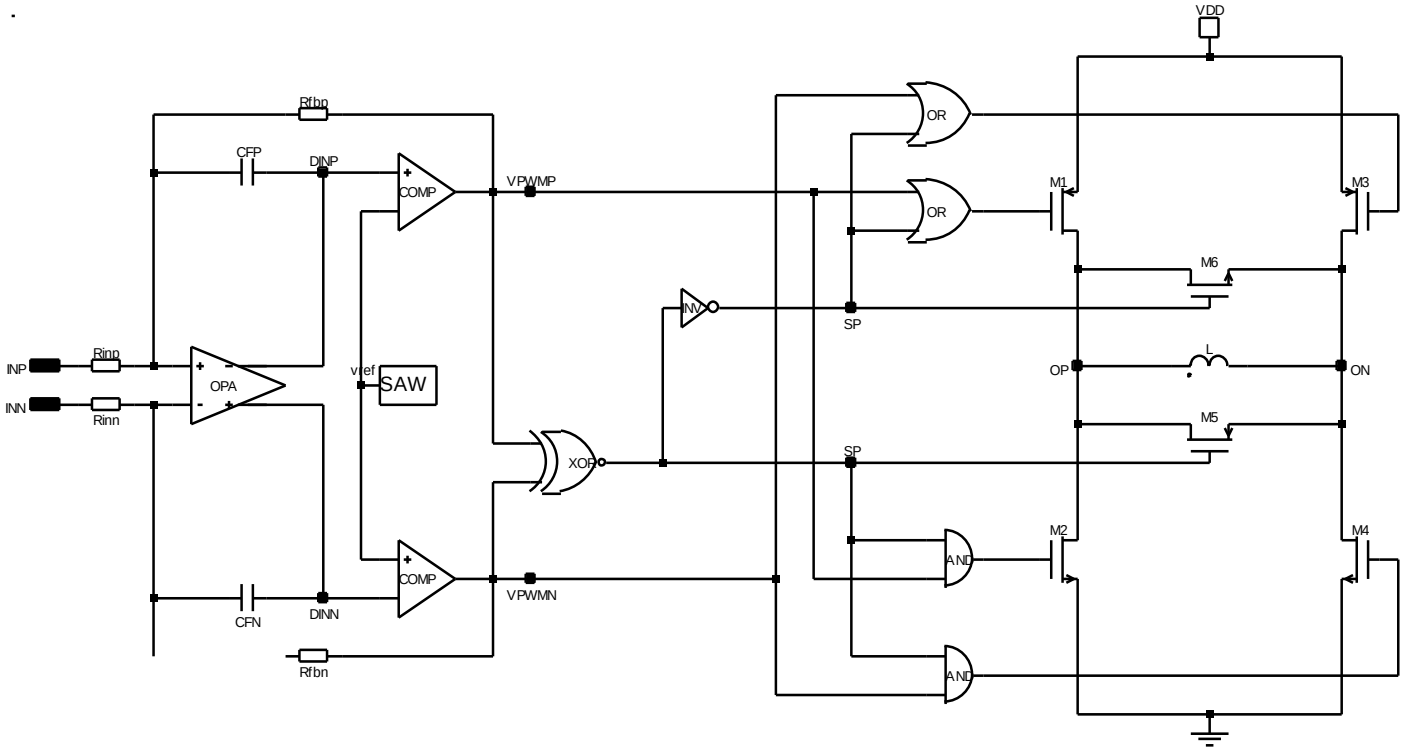

Fig. 2. The proposed class-D amplifier.

triangle-wave generator which is used to generate the Vclk and triangle wave signal Vtrangle for the PWM control. The last part is the driver circuit usually includes a control circuit, an H-Bridge driver or H-bridge, and a pulse width modulated (PWM) circuit that converts the analog signal from amplifier to a first pulse width modulated (PWM) signal or positive PWM signal (DP) and a second PWM signal or negative PWM signal (DN). The PWM circuit typically includes a sawtooth signal (SWA) generator, a first comparator and a second comparator that is configured to receive the analog signal from input amplifier, receive the sawtooth signal from saw, and form the respective DP and DN signals. Driver Circuit utilizes the two PWM signals (DP and DN) to control the H-Bridge. The H-bridge includes two pair of series connected switches. The first pair of series connected switches is configured in a totem pole configuration, such as illustrated by a first transistor M1 and a second transistor M2. A common connection between the two switches forms the OP signal and is connected to output. The second pair of series connected switches are also configured in a totem pole configuration, such as illustrated by a third transistor M3 and a fourth transistor M4. The second pair of series connected switches also has a common connection between the two switches that forms the ON signal and is connected to output. The H-bridge is connected between input supply voltage such as a battery and ground in order to connect load to receive current from the input voltage and conduct the current to ground. Control circuit includes an exclusive OR (XOR) gate, an inverter, tow OR gates, tow AND gates, and a shorting switch that is connected between the two common connections of the H-Bridge. For example illustrated in figure.2, the shorting switch is implemented as two parallel transistors M5 and M6. The two transistors are used for the switch to ensure bi-directional current flow between the two common points of the H-Bridge. Control circuit forms a positive switch signal (SP) and a negative switch signal (SN) that are used to control the switch of respective

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transistors M5 and M6. As will be seen further hereinafter, control circuit is operably coupled to inhibit supplying current to or sinking current from outputs OP and ON and also holds outputs OP and ON at a voltage value that is greater than the voltage on ground and lower than the voltage supply.

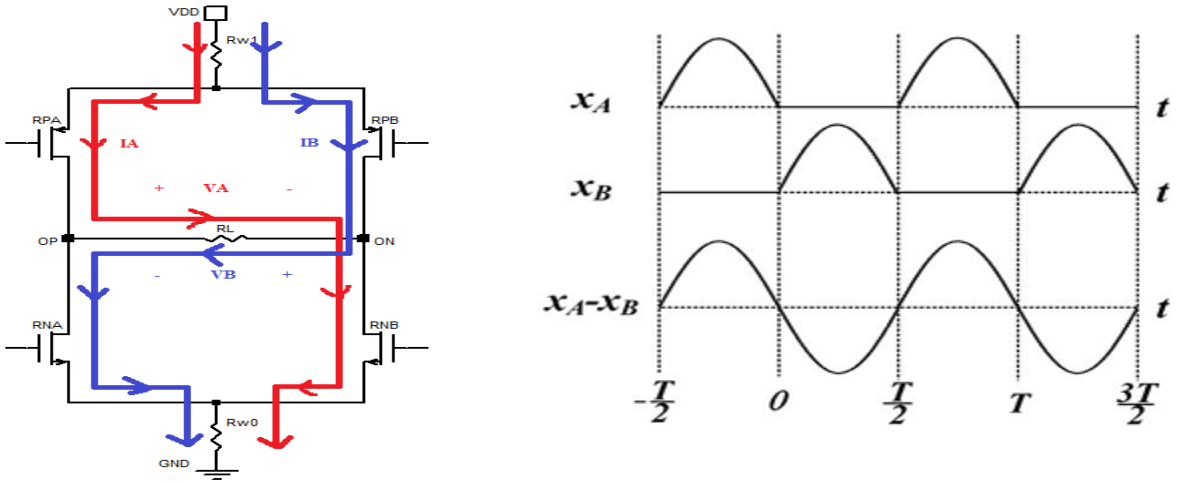

Fig. 3. The H-bridge power stage and the relationship between xA, xB and (xA-xB) in time domain.

As shown in Fig.3, a typical H-bridge is composed of half bridges A and B. Each contains a power PMOS and a power NMOS. Rw1 and Rw0 are the parasitic resistances in the supply rail and the ground path, respectively, while RPA, RPB, RNA and RNB are the respective on-resistances of the power MOSFETs M1, M2, M3 and M4. For the half-bridge, the turned-on and turned-off PWM duty cycle will induce different inductor current paths. The current path of the turned-on duty of half-bridge starts from VDD, passes through Rw1, RPA, load resistance RL, and RNB, and Rw0, and ends at GND. The turned-off current path starts from the on-chip GND, flows through RNA, RL, RNB, and then returns to the on-chip GND. When the duty is turned-on and turned-off, the voltage of node OP can be respectively expressed as $V_{A,on} = VDD - I_A.(R_{w1} + R_{PA} + R_{NB} + R_{W0})$ and $V_{A,off} = -I_A.(R_{NB} + R_{NA})$ where IA is the average output current for driving the loud speaker load RL. In a switching cycle, the average voltage at node OP, denoted as vA can be expressed as

$$v_A = x_A.V_{A.on} + (1 - x_A).V_{A.off} \quad (1)$$

Where xA is the turned-on duty-cycle of the PWM output. By substituting VA.ON and VA.OFF into (1) and replacing IA with vA/RL, We can obtain

$$v_A = \frac{c_2.x_A}{1 + c_1.x_A}.VDD \quad (2)$$

Where $c_1 = (R_{w1} + R_{PA} + R_{w0} - R_{NA})/(R_L + R_{NA} + R_{NB})$

And $c_2 = R_L(R_L + R_{NA} + R_{NB})$. since the duty-cycle xA is 0~1 and c1 << 1, by applying a Taylor-series expansion, (2) can be rewritten as

$$v_A = c_2.x_A.VDD.(1 - c_1x_A + c_1^2x_A^2 - \cdots). \quad (3)$$

The duty-cycle xA for half-bridge P changes with the signal Level of the audio input. With the ternary-PWM, the differential signal xA-xB of a sinusoidal input is plotted in Fig. 3. The signal xA is active during $-\pi/2 \sim \pi/2$, while xB is active during $\pi/2 \sim 3\pi/2$. By using the Fourier series expansion,

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xA can be expressed as

$$x_A = M.\left[\frac{1}{\pi}+\frac{1}{2}.\cos\omega t-\frac{2}{\pi}\sum_{n=2,4,\dots}^{\infty}\frac{\cos\left(\frac{n\pi}{2}\right)}{n^2-1}.\cos\omega t\right] \quad (4)$$

Where ω and M are the radian frequency and the modulation index, respectively. Replacing in (3) with (4), the coefficients of the cosωt, cos2ωt and cso3ωt terms can be obtained. With a similar derivation, the average voltage of ON, which is denoted as vB, can be obtained. The differential signal on the load RL can be obtained by (vA-vB). After eliminating negligible high-order terms, the second and third harmonic distortions, HD2 and HD3, can be respectively expressed as

$$HD_2 \approx \left(\frac{1}{8}+\frac{4}{4\pi^2}\right).\left(\frac{R_{PB}-R_{PA}+R_{NA}-R_{NB}}{R_L+R_{NA}+R_{NB}}\right).M \quad (5)$$

And

$$HD_3 \approx \left[\frac{R_{PA}-R_{NA}+R_{PB}-R_{NB}+2R_{w1}+2R_{w0}}{R_L+R_{NA}+R_{NB}}\right].M \quad (6)$$

As in (5), HD2 of the open-loop switching power stage is determined by the mismatch of the power transistors, and thus can be minimized by a carefully matched layout design. In (6), the quantitative analysis on HD3 versus Rw1 and Rw0 is shown and can be referred to the supply voltage modulation effect.

B. Ttriangular-wave generator circuit

The adaptive triangle-wave generator is shown in Fig. 4[9]. The switching frequency can be adjusted by VREF of modified pulse-width modulation. It is used to generate the clock signal VCLK and triangle wave signal VTRIANGLE for the PWM control. The triangular-wave generator contains current generator and two hysteresis voltage comparator. The reference voltage VREF passes through operational amplifier and RT to produce current ID1 as $I_{D1}=\frac{V_{ref}}{R_T}$ (7) . Using W/L of MP1 and MP3 $I_{D1}=K.I_{D2}=I_{D3}$ (8)

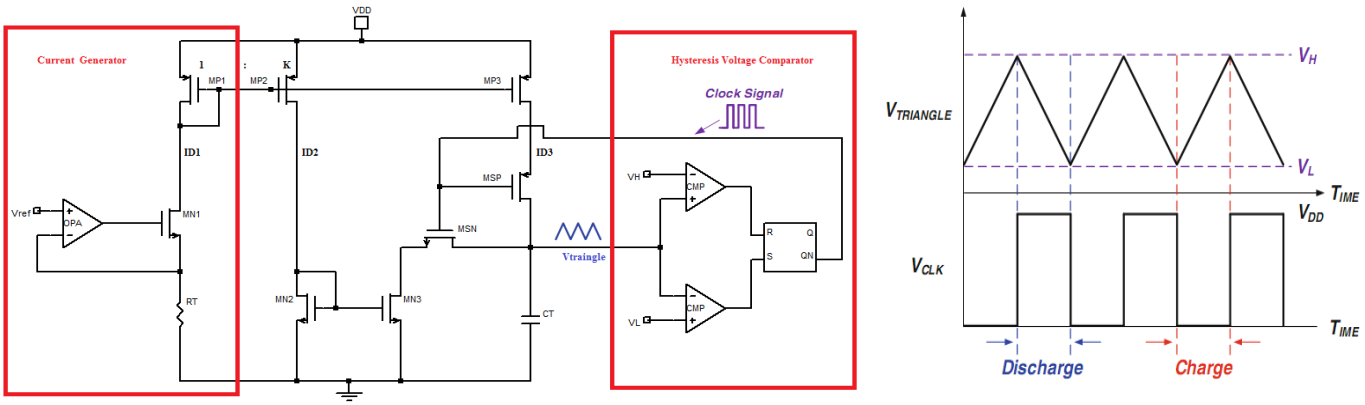

Fig. 4. The adaptive triangular-wave generator circuit

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The signal of the triangular-wave generator produces a pulse signal through the clock signal VCLK to determent the on/off state of transistors MSP and MSN. The amplitude of VTRIANGLE is VPWM. The hysteresis window VPWM =VH - VL has been set to 1V. When VTRIANGLE < VL the clock signal VCLK can be considered as logical low, and the current ID3 will charge the capacitor CT. Similarly, when VTRIANGLE >VH the clock signal VCLK can be considered as logical high, and MSN will discharge the capacitor CT. The hysteresis voltage comparator circuits from VH, VL and VTRIANGLE produces the hysteresis interval from upper limits of VH and lower limits of VL. It can limit the signal of VTRIANGLE to produce two signals into the RS-Latch flip-flop. The RS-Latch flip-flop can produce square wave signal VCLK. In order to reduce switching loss in the power stage and obtain a more precise PWM signal, we set the switching frequency to 1MHz.

The efficiency and distortion performance can be modified. The FVRIANGLET can be written as

$$\mathrm{F\_VTRANGLE} = 1/(\mathrm{T\_charge} + \mathrm{T\_decharge} \qquad (9)$$

With

$$\mathrm{T_{charge}} = \mathrm{C_T}(\mathrm{V_H} - \mathrm{V_L})\mathrm{I_{D3}} \qquad (10)$$

$$T_{decharge} = C_T(V_H - V_L)I_{D2} \qquad (11)$$

C. Comparator circuit

The comparator used in the design is shown in Fig. 5 [10].It is implemented by three stages. The first stage has a p- channel differential input pair with the positive feedback circuit. The second stage has a n-channel differential input pair with a p-channel current mirror active load. The third stage is an inverter chain.

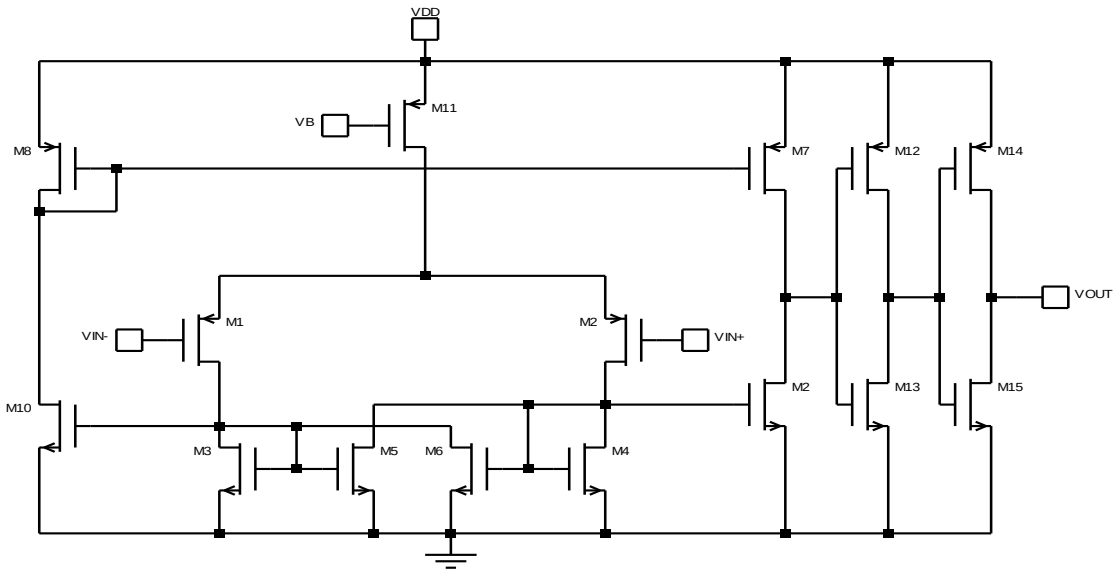

Fig. 5. The comparator circuit

The transistors of M3, M4, M5, and M6 form the positive feedback gain stage. The gain of the positive gain stage is given by $\mathrm{A_V} = \sqrt{\frac{\mu_{\mathrm{p}}(\frac{\mathrm{W}}{\mathrm{L}})_1}{\mu_{\mathrm{n}}(\frac{\mathrm{W}}{\mathrm{L}})_3}} * \frac{1}{1-\alpha}$ (12).

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Where $\alpha = (w/L)_5/(w/L)_3$

The transistors of M7, M8, M9, and M10 constitute the second stage. This stage mainly contributes some gain in whole circuit. The gain of the second stage is as following

$$A\_V2 = g\_m10 \times ((r\_ds7//r\_ds10) \qquad (13)$$

The third stage constituted by the inverter chain M12, M13, M14, and M15, are used to increase the response of output signal. With the usage of this stage, the size of M9 and M10 can be reduced to achieve same performance and due to the reduction of M9 and M10, the effect of the parasitic capacitance at gates of M7 and M8 is decreased which results in a faster response.

D. Analog amplifier with common-mode feedback circuit

The circuit diagram of a fully differential amplifier with common-mode feedback (CMFB) circuit is shown in Fig. 6. The key sub-circuit is fully cascade differential amplifier which consists of M1 to M11.The output terminals of VOUTP and VOUTN are influenced by processes easily. The operation point of the circuit may be shifted. So, using common-mode feedback circuit can regulate the operation point of VOUTP and VOUTN. When the common mode voltage of VOUTP and VOUTN is not equal to VCM, the bias current can be generated by the voltage difference of M12–M14 and M16–M18.Then,this bias current through M15, M11 and M10 mirrors the fully cascade differential amplifier, it let the common-mode voltage level of VOUTP and VOUTN return to the voltage of VCM. The fully differential amplifier has a dc gain of 64dB and gain band width product (GBW) around 316MHz.

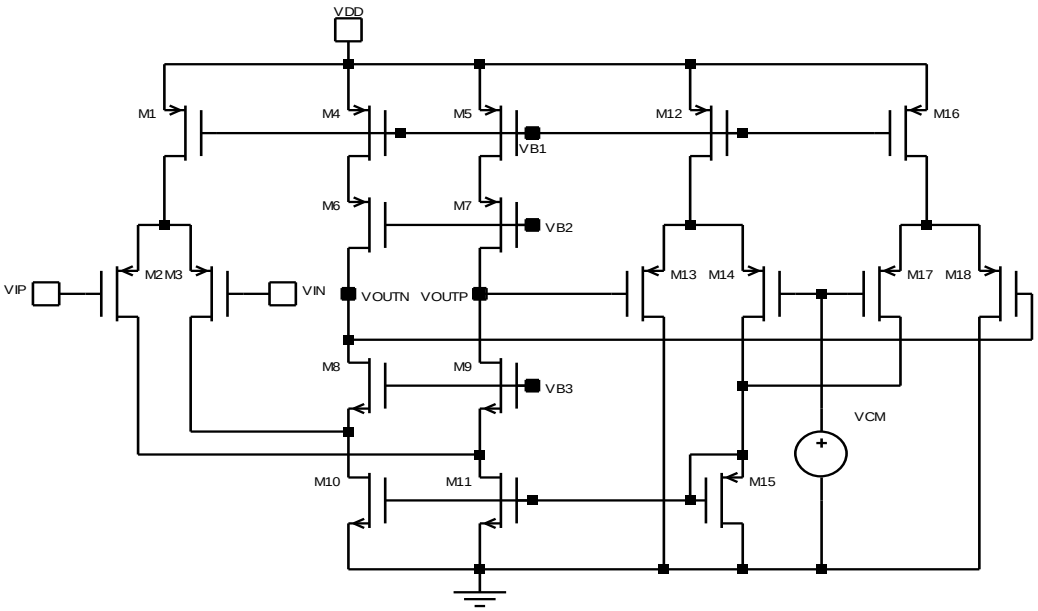

Fig. 6. Analog amplifier with CMFB citcuit

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III. SIMULATION RESULTS

A. Efficiency and Output Power

The efficiency versus power curve for1-kHz input signal at different supply voltages is shown in Fig.7. The results show that the proposed class D audio amplifier has very high efficiency, reaching a maximum power efficiency of 95% for a 5V supply voltage.

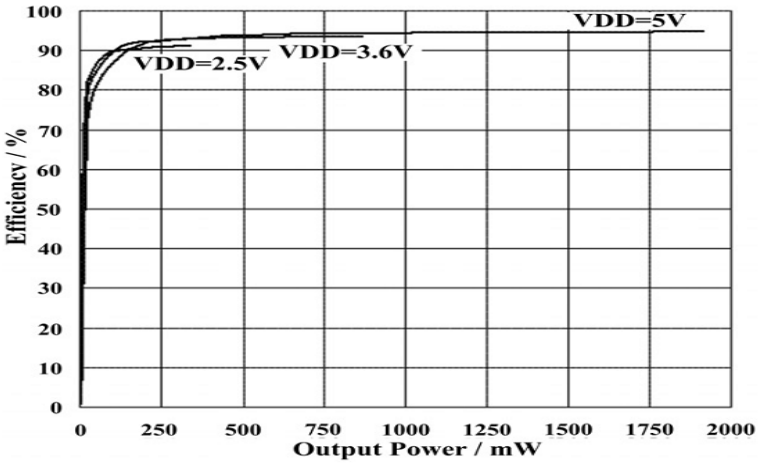

Fig. 7. Efficiency versus power curve

B. THD+N

The THD+N was simulated with an audio precision (AP) system. A low-pass filter had to be used at the output since the AP system cannot handle pure class D audio amplifiers because of the high-frequency PWM wave form. Fig.8 shows a plot of the THD+N versus frequency for output power 0.4W. The results show that the THD+N is below 0.2% in the normal output power ranging from 0.1to1W.

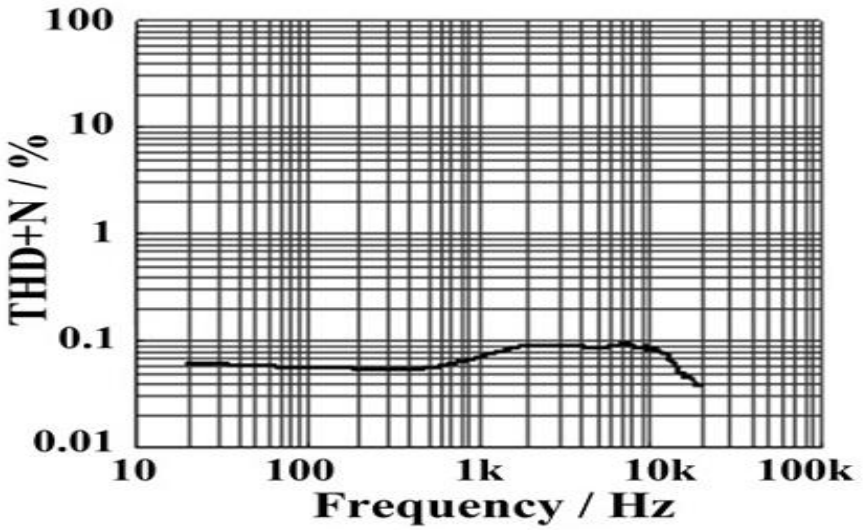

Fig. 8. THD+N versus frequency with output power of 0.4W.

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C. Layout

The Layout of the proposed class D audio amplfier is circuit is shown in Fig. 9. Layout techniques such as guard rings and careful power and ground routing can minimize the spikes induced onto the sensitive linear sections.

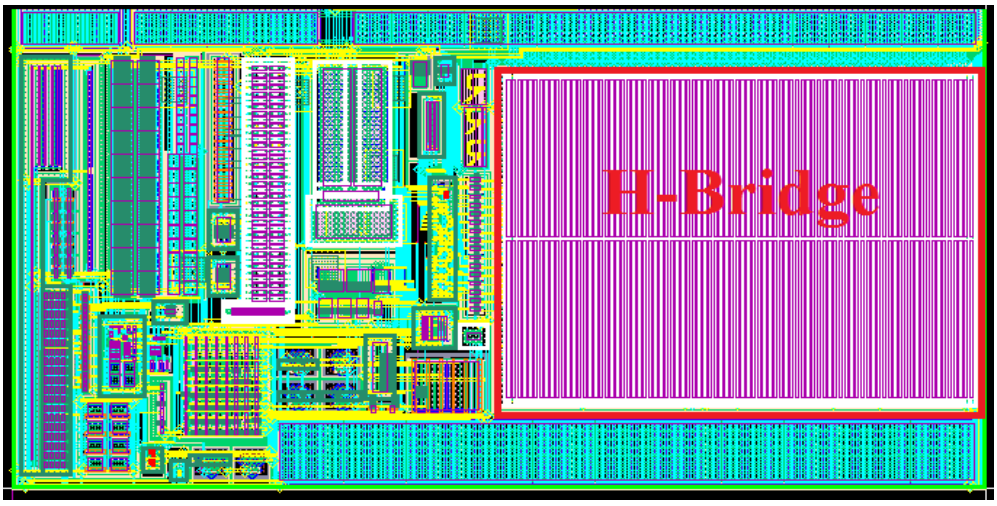

Fig. 9. Layout of Class D (325um x300 um = 0.1mm2)

IV. CONCLUSIONS

We have presented a new class D audio amplifier for low voltage applications with high efficiency and minimum system solution size. The class D amplifier was implemented with TSMC 0.13-um 2P4M CMOS process. With the switching frequency of 1MHz, the proposed class-D amplifier achieves 0.029% THD and efficiency of 95%. Simulation results demonstrate good linearity and low distortion. The proposed class-D amplifier is suitable for portable devices application.

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